BACKPLANES

PCI/ISA
PCI-X

No. 87-001036-000 Revision N

TECHNICAL REFERENCE

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Serial number from the label on the back of the product
Description of the failure

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HANDLING PRECAUTIONS

WARNING: This product has components which may be damaged by electrostatic discharge.

To protect your backplane from electrostatic damage, be sure to observe the following precautions when handling or storing the backplane:

- Keep the backplane in its static-shielded bag until you are ready to perform your installation.
- Handle the backplane by its edges.
- Do not touch the I/O connector pins. Do not apply pressure or attach labels to the backplane.
- Use a grounded wrist strap at your workstation or ground yourself frequently by touching the metal chassis of the system before handling any components. The system must be plugged into an outlet that is connected to an earth ground.
- Use antistatic padding on all work surfaces.
- Avoid static-inducing carpeted areas.

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Chapter 1 Backplane Overview

INTRODUCTION

Trenton backplanes are six-layer or eight-layer backplanes which allow the use of standard ISA, PCI or PCI-X option cards. Types and numbers of option cards supported vary depending on the backplane model.

MODELS

Model #	Model Name	Description
PCI Backplanes:		
5457-000	BP3/16	3 ISA, 16 PCI Slots
5491-000	BP7/6	7 ISA, 6 PCI Slots
5495-000	BP13/6	13 ISA, 6 PCI Slots
5498-000	BP17/3	17 ISA, 3 PCI Slots
5501-000	BP11/3	11 ISA, 3 PCI Slots
5504-000	BP5/3	5 ISA, 3 PCI Slots
5635-000	BP8/12	8 ISA, 12 PCI Slots
5937-000	BP3/10	3 ISA, 10 PCI Slots
64-bit Backplanes:		
5693-000	BP13/6-64	19 Slots - 13 ISA, 6 64-bit/33MHz PCI
5696-000	BP3/16-64	19 Slots - 3 ISA, 16 64-bit/33MHz PCI
5786-000	BP13/2/4-66	19 Slots - 13 ISA, 2 64-bit/66MHz PCI, 4 64-bit/33MHz PCI
5951-000	BP3/2/4/4	13 Slots - 3 ISA, 2 64-bit/66MHz PCI, 4 64-bit/33MHz PCI, 4 32-bit/33MHz PCI
5971-000	BP1/2	3 Slots - 1 SBC Slot, 2 64-bit/33MHz PCI
6195-000	BP3/6/4	13 Slots - 3 ISA, 6 64-bit/66MHz PCI, 4 64-bit/33MHz PCI
Segmented Backplanes:		
5574-000	BP2S13	13- Slot Segmented - 4 ISA/3 PCI and 3 ISA/3 PCI
5577-000	BP2S19	19- Slot Segmented - 7 ISA/3 PCI and 6 ISA/3 PCI
PCI-X Backplane:		
6120-000	BP1/1/2/4/4	12 Slots - 1 SBC Slot, 1 PCI-X 64-bit/133MHz, 2 PCI-X 64-bit/100MHz, 4 PCI-X 64-bit/66MHz, 4 PCI 64-bit/33MHz

FEATURES

- Six-layer or eight-layer printed circuit board
- High noise immunity construction
- Accept single board computers (SBCs) with PCI Industrial Computer Manufacturers Group (PICMG®) 1.0 compatible PCI Local Bus extension and standard ISA Bus SBCs, depending on model
- Allow use of standard ISA, PCI or PCI-X option cards, depending on model
- Bus termination resistor sockets
- Standard AT, ATX, extended-current and/or EPS power connectors, depending on model

BACKPLANE OVERVIEW

Bus Architecture

The PCI/ISA backplanes allow the use of standard ISA Bus and PCI Local Bus option cards. The backplanes accept SBCs with PICMG compliant PCI Local Bus extension connectors to route the local bus signals to the standard PCI Local Bus expansion slots. The backplanes also accept standard ISA Bus SBCs. The PCI-X backplanes provide support for PCI-X and PCI option cards.

Each backplane is described individually in the following chapters of this manual.

Bus Terminations - ISA Bus

Terminations provide a method to prevent or minimize reflections and interference on the bus. If a bus is not terminated, the bus signals reach the end of the bus and reflect back down the bus. In extreme cases, these reflected signals interfere with the real bus information, leading to spurious operation or lock-ups. This can become a significant factor on the ISA Bus with option cards having non-standard load characteristics or with long ISA Bus lengths. However, provision is made for installing terminations as required by the customer's application.

The backplanes provide termination sockets at the left end of the bus for the ISA Bus.

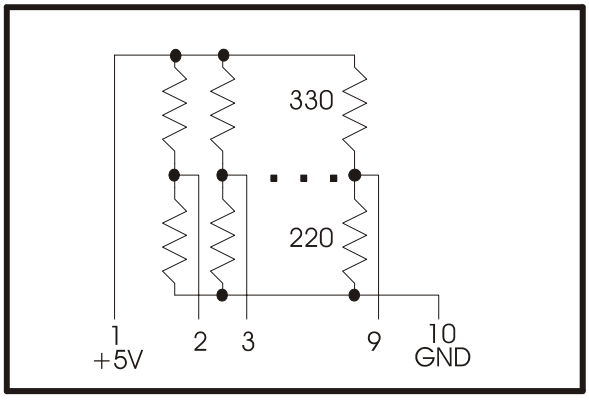
Terminations connect the bus to +5V and ground, providing a path for the bus signals to dissipate. A terminated bus provides signals with less noise, but the rise and fall times are slower. However, this is highly dependent on the SBC and option cards and must be evaluated on a case-by-case basis.

The sockets provided on the backplane accept standard 10-position SIPs manufactured by Bourns and others. Signals and corresponding termination connections are listed later in this chapter.

Resistor Termination

The goal of terminating resistors is to provide an impedance mismatch at the end of the bus to prevent the signal reflections. This mismatch has to be balanced by the capability of the SBC and option cards to electrically drive the load imposed by the resistors.

An illustration of the Resistor SIP Network is shown below:



Resistor SIP Network

Generally, terminations which connect to both +5V and ground work best, although terminations to +5V only are possible.

A good compromise in digital systems is a resistor network connected to both +5V and ground as follows:

Bourns part #4610X-104-331/471 (low profile)
Bourns part #4610M-104-331/471 (medium profile)

330 ohms to +5V
470 ohms to ground

Another combination which frequently works but provides more bus loading is as follows:

Bourns part #4610X-104-221/331 (low profile)
Bourns part #4610M-104-221/331 (medium profile)

220 ohms to +5V
330 ohms to ground

Other values are manufactured and can be used if a problem persists on the bus. Not all cards behave well on large buses or in combination with other cards and may require some experimentation to completely isolate all intermittent operation. Turning the SIP around is also allowed.

Reading the resistance from the signal pin of the SIP to either pin 1 or pin 10 will not provide the expected resistance of 220 ohms or 330 ohms, for example. This is because of the parallel resistance of the other paths. For example, the 220 ohm side will ideally read 140.8 ohms and the 330 ohm side will read 151.8 ohms. The actual values will change slightly because of allowed tolerance.

Keyboard Connectors

For those backplanes with keyboard connectors, there are three keyboard connectors connected in parallel on the backplanes. Two are 5-pin headers and one is a standard AT 5-pin DIN connector. One of the two 5-pin headers may be used to bring keyboard signals from the SBC to the backplane and the other to provide a front-mounted keyboard connector. The 5-pin DIN provides a standard back panel connector. In addition, provision has been made for optional filtering for the 5-pin DIN connector when necessary. (Refer to the backplane block diagrams in the following chapters of this manual.)

Power Supply Connectors

Many backplanes have multiple power supply connectors. On these backplanes, the +5V connections are generally common, as are all of the +12V, -12V, +5V and ground connections. Power may be connected via any of the connectors, as long as all four voltages are delivered to the system.

Trenton backplanes provide +3.3V power supply connections for PCI peripheral cards which require +3.3V of DC power. Trenton Technology SBCs do not require +3.3 volts from the power supply because they have their own VRMs on board. The +3.3V power supply connections do *not* power the processor slot on these backplanes.

Some models provide optional ATX, extended-current or EPS power connectors. Refer to the backplane descriptions in the following chapters of this manual for more information about a specific backplane.

TERMINATOR RESISTOR SIGNAL ASSIGNMENTS

Resistor Network 1/101

Pin	ISA Pin	Signal Name
1		+5V
2	A9	SD0
3	A8	SD1
4	A7	SD2
5	A6	SD3
6	A5	SD4
7	A4	SD5
8	A3	SD6
9	A2	SD7
10		Gnd

Resistor Network 2/102

Pin	ISA Pin	Signal Name
1		+5V
2	A10	CHRDY
3	B8	NOWS#
4	A11	AEN
5	B6	DRQ2
6		NC
7	B4	IRQ9
8	A1	IOCHK#
9	B2	RESDRV
10		Gnd

Resistor Network 3/103

Pin	ISA Pin	Signal Name
1		+5V
2	A15	SA16
3	A14	SA17
4	A13	SA18
5	B13	IOWC#
6	B12	SMRDC#
7	B11	SMWTC#
8	A12	SA19
9		NC
10		Gnd

Resistor Network 4/104

Pin	ISA Pin	Signal Name
1		+5V
2	B21	IRQ7
3	B20	BCLK
4	B19	REFRESH#
5	B18	DRQ1
6	B17	DAK1#
7	B16	DRQ3
8	B15	DAK3#
9	B14	IORC#
10		Gnd

Resistor Network 5/105

Pin	ISA Pin	Signal Name
1		+5V
2	A23	SA8
3	A22	SA9
4	A21	SA10
5	A20	SA11
6	A19	SA12
7	A18	SA13
8	A17	SA14
9	A16	SA15
10		Gnd

Resistor Network 6/106

Pin	ISA Pin	Signal Name
1		+5V
2	B30	OSC
3	B28	BALE
4	B27	T-C
5	B26	DAK2#
6	B25	IRQ3
7	B24	IRQ4
8	B23	IRQ5
9	B22	IRQ6
10		Gnd

TERMINATOR RESISTOR SIGNAL ASSIGNMENTS (CONTINUED)

Resistor Network 7/107

Pin	ISA Pin	Signal Name
1		+5V
2	A31	SA0
3	A30	SA1
4	A29	SA2
5	A28	SA3
6	A27	SA4
7	A26	SA5
8	A25	SA6
9	A24	SA7
10		Gnd

Resistor Network 8/108

Pin	ISA Pin	Signal Name
1		+5V
2	D8	DAK0#
3	D7	IRQ14
4	D6	IRQ15
5	D5	IRQ12
6	D4	IRQ11
7	D3	IRQ10
8	D2	IO16#
9	D1	M16#
10		Gnd

Resistor Network 9/109

Pin	ISA Pin	Signal Name
1		+5V
2	C8	LA17
3	C7	LA18
4	C6	LA19
5	C5	LA20
6	C4	LA21
7	C3	LA22
8	C2	LA23
9	C1	SBHE#
10		Gnd

Resistor Network 10/110

Pin	ISA Pin	Signal Name
1		+5V
2		NC
3		NC
4	C11	SD8
5	C10	MWTC#
6	D10	DAK5#
7	D9	DRQ0
8	C9	MRDC#
9		NC
10		Gnd

Resistor Network 11/111

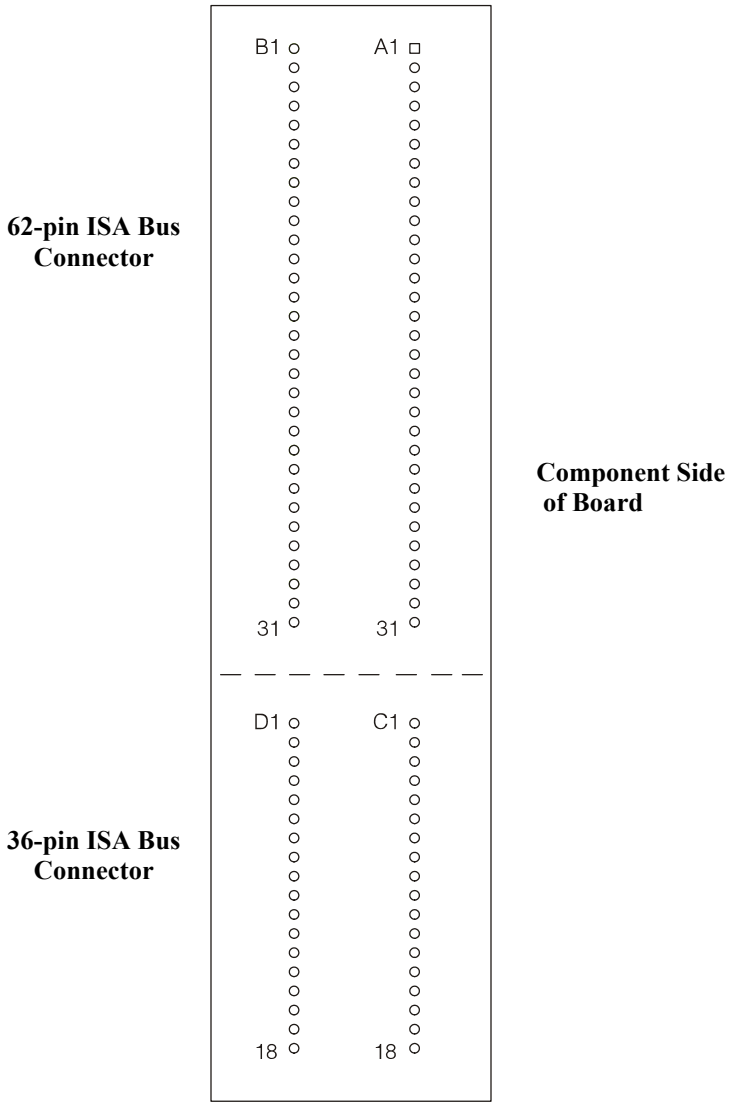
Pin	ISA Pin	Signal Name
1		+5V
2		NC
3	C18	SD15
4	C17	SD14
5	C16	SD13
6	C15	SD12
7	C14	SD11
8	C13	SD10
9	C12	SD9
10		Gnd

Resistor Network 6/106

Pin	ISA Pin	Signal Name
1		+5V
2		NC
3		NC
4	D17	Master16#
5	D15	DRQ7
6	D14	DAK7#
7	D13	DRQ6
8	D12	DAK6#
9	D11	DRQ5
10		Gnd

Chapter 2 ISA/PCI Reference

ISA BUS PIN NUMBERING



ISA BUS PIN ASSIGNMENTS

The following tables summarize pin assignments for the Industry Standard Architecture (ISA) Bus connectors.

I/O Pin	Signal Name	I/O	I/O Pin	Signal Name	I/O
A1	IOCHK#	I	B1	Gnd	Ground
A2	D7	I/O	B2	RESDRV	O
A3	D6	I/O	B3	+5V	Power
A4	D5	I/O	B4	IRQ9	I
A5	D4	I/O	B5	-5V	Power
A6	D3	I/O	B6	DRQ2	I
A7	D2	I/O	B7	-12V	Power
A8	D1	I/O	B8	NOWS#	I
A9	D0	I/O	B9	+12V	Power
A10	CHRDY	I	B10	Gnd	Ground
A11	AEN	O	B11	SMWTC#	O
A12	SA19	I/O	B12	SMRDC#	O
A13	SA18	I/O	B13	IOWC#	I/O
A14	SA17	I/O	B14	IORC#	I/O
A15	SA16	I/O	B15	DAK3#	O
A16	SA15	I/O	B16	DRQ3	I
A17	SA14	I/O	B17	DAK1#	O
A18	SA13	I/O	B18	DRQ1	I
A19	SA12	I/O	B19	REFRESH#	I/O
A20	SA11	I/O	B20	BCLK	O
A21	SA10	I/O	B21	IRQ7	I
A22	SA9	I/O	B22	IRQ6	I
A23	SA8	I/O	B23	IRQ5	I
A24	SA7	I/O	B24	IRQ4	I
A25	SA6	I/O	B25	IRQ3	I
A26	SA5	I/O	B26	DAK2#	O
A27	SA4	I/O	B27	T-C	O
A28	SA3	I/O	B28	BALE	O
A29	SA2	I/O	B29	+5V	Power
A30	SA1	I/O	B30	OSC	O
A31	SA0	I/O	B31	Gnd	Ground

I/O Pin	Signal Name	I/O	I/O Pin	Signal Name	I/O
C1	SBHE#	I/O	D1	M16#	I
C2	LA23	I/O	D2	IO16#	I
C3	LA22	I/O	D3	IRQ10	I
C4	LA21	I/O	D4	IRQ11	I
C5	LA20	I/O	D5	IRQ12	I
C6	LA19	I/O	D6	IRQ15	I
C7	LA18	I/O	D7	IRQ14	I
C8	LA17	I/O	D8	DAK0#	O
C9	MRDC#	I/O	D9	DRQ0	I
C10	MWTC#	I/O	D10	DAK5#	O
C11	D8	I/O	D11	DRQ5	I
C12	D9	I/O	D12	DAK6#	O
C13	D10	I/O	D13	DRQ6	I
C14	D11	I/O	D14	DAK7#	O
C15	D12	I/O	D15	DRQ7	I
C16	D13	I/O	D16	+5V	Power
C17	D14	I/O	D17	Master16#	I
C18	D15	I/O	D18	Gnd	Ground

ISA BUS SIGNAL DESCRIPTIONS

The following is a description of the ISA Bus signals. All signal lines are TTL-compatible.

AEN (O)

Address Enable (AEN) is used to degate the microprocessor and other devices from the I/O channel to allow DMA transfers to take place. When this line is active, the DMA controller has control of the address bus, the data-bus Read command lines (memory and I/O), and the Write command lines (memory and I/O).

BALE (O) (Buffered)

Address Latch Enable (BALE) is provided by the bus controller and is used on the system board to latch valid addresses and memory decodes from the microprocessor. It is available to the I/O channel as an indicator of a valid microprocessor or DMA address (when used with AEN). Microprocessor addresses SA[19::0] are latched with the falling edge of BALE. BALE is forced high during DMA cycles.

BCLK (O)

BCLK is the system clock. The clock has a 50% duty cycle. This signal should only be used for synchronization. It is not intended for uses requiring a fixed frequency.

CHRDY (I)

I/O Channel Ready (CHRDY) is pulled low (not ready) by a memory or I/O device to lengthen I/O or memory cycles. Any slow device using this line should drive it low immediately upon detecting its valid address and a Read or Write command. Machine cycles are extended by an integral number of clock cycles. This signal should be held low for no more than 2.5 micro-seconds.

D[15::0] (I/O)

Data signals D[15::0] provide bus bits 15 through 0 for the microprocessor, memory, and I/O devices. D15 is the most-significant bit and D0 is the least-significant bit. All 8-bit devices on the I/O channel should use D[7::0] for communications to the microprocessor. The 16-bit devices will use D[15::0]. To support 8-bit devices, the data on D[15::8] will be gated to D[7::0] during 8-bit transfers to these devices. 16-bit microprocessor transfers to 8-bit devices will be converted to two 8-bit transfers.

DAK[7::5]#, DAK[3::0]# (O)

DMA Acknowledge DAK[7::5]# and DAK[3::0]# are used to acknowledge DMA requests DRQ[7::5] and DRQ[3::0]. They are active low.

DRQ[7::5], DRQ[3::0] (I)

DMA Requests DRQ[7::5] and DRQ[3::0] are asynchronous channel requests used by peripheral devices and the I/O channel microprocessors to gain DMA service (or control of the system). They are prioritized, with DRQ0 having the highest priority and DRQ7 having the lowest. A request is generated by bringing a DRQ line to an active level. A DRQ line must be held high until the corresponding DMA Request Acknowledge (DAK) line goes active. DRQ[3::0] will perform 8-bit DMA transfers; DRQ[7::5] will perform 16-bit transfers.

IO16# (I)

I/O 16-bit Chip Select (IO16#) signals the system board that the present data transfer is a 16-bit, 1 wait-state, I/O cycle. It is derived from an address decode. IO16# is active low and should be driven with an open collector or tri-state driver capable of sinking 20 mAmps.

IOCHK# (I)

I/O Channel Check (IOCHK#) provides the system board with parity (error) information about memory or devices on the I/O channel. When this signal is active, it indicates an uncorrectable system error.

IORC# (I/O)

I/O Read (IORC#) instructs an I/O device to drive its data onto the data bus. It may be driven by the system microprocessor or DMA controller, or by a microprocessor or DMA controller resident on the I/O channel. This signal is active low.

IOWC# (I/O)

I/O Write (IOWC#) instructs an I/O device to read the data on the data bus. It may be driven by any microprocessor or DMA controller in the system. This signal is active low.

IRQ[15::14], IRQ[12::9], IRQ[7::3] (I)

Interrupt Requests IRQ[15::14], IRQ[12::9] and IRQ[7::3] are used to signal the microprocessor that an I/O device needs attention. The interrupt requests are prioritized, with IRQ[15::14] and IRQ[12::9] having the highest priority (IRQ9 is the highest) and IRQ[7::3] having the lowest priority (IRQ7 is the lowest). An interrupt request is generated when an IRQ line is raised from low to high. The line must be held high until the microprocessor acknowledges the interrupt request (Interrupt Service routine).

LA[23::17] (I/O)

These signals (unlatched) are used to address memory and I/O devices within the system. They give the system up to 16MB of addressability. These signals are valid when BALE is high. LA[23::17] are not latched during microprocessor cycles and therefore do not stay valid for the whole cycle. Their purpose is to generate memory decodes for 1 wait-state memory cycles. These decodes should be latched by I/O adapters on the falling edge of BALE. These signals also may be driven by other microprocessors or DMA controllers that reside on the I/O channel.

M16# (I)

M16# Chip Select signals the system board if the present data transfer is a 1<N>wait-state, 16-bit, memory cycle. It must be derived from the decode of LA[23::17]. M16# should be driven with an open collector or tri-state driver capable of sinking 20 mAmps.

Master16# (I)

Master16# is used with a DRQ line to gain control of the system. A processor or DMA controller on the I/O channel may issue a DRQ to a DMA channel in cascade mode and receive a DAK#. Upon receiving the DAK#, an I/O microprocessor may pull Master16# low, which will allow it to control the system address, data, and control lines (a condition known as tri-state). After Master16# is low, the I/O microprocessor must wait one system clock period before driving the address and data lines, and two clock periods before issuing a Read or Write command. If this signal is held low for more than 15<N>microseconds, system memory may be lost because of a lack of refresh.

NOWS# (I)

The No Wait State (NOWS#) signal tells the microprocessor that it can complete the present bus cycle without inserting any additional wait cycles. In order to run a memory cycle to a 16-bit device without wait cycles, NOWS# is derived from an address decode gated with a Read or Write command. In order to run a memory cycle to an 8-bit device with a minimum of two wait states, NOWS# should be driven active on system clock after the Read or Write command is active gated with the address decode for the device. Memory Read and Write commands to a 8-bit device are active on the falling edge of the system clock. NOWS# is active low and should be driven with an open collector or tri-state driver capable of sinking 20 mAmps.

OSC (O)

Oscillator (OSC) is a high-speed clock with a 70-nanosecond period (14.31818 MHz). This signal is not synchronous with the system clock. It has a 50% duty cycle.

REFRESH# (I/O)

The REFRESH# signal is used to indicate a refresh cycle and can be driven by a microprocessor on the I/O channel.

RESDRV (O)

Reset Drive (RESDRV) is used to reset or initialize system logic at power-up time or during a low line-voltage outage. This signal is active high.

SA[19::0] (I/O)

Address bits SA[19::0] are used to address memory and I/O devices within the system. These twenty address lines, in addition to LA[23::17], allow access of up to 16MB of memory. SA[19::0] are gated on the system bus when BALE is high and are latched on the falling edge of BALE. These signals are generated by the microprocessor or DMA Controller. They also may be driven by other microprocessors or DMA controllers that reside on the I/O channel.

SBHE# (I/O)

System Bus High Enable (SBHE#) indicates a transfer of data on the upper byte of the data bus, D[15::8]. 16-bit devices use SBHE# to condition data bus buffers tied to D[15::8].

SMRDC# (O), MRDC# (I/O)

These signals instruct the memory devices to drive data onto the data bus. SMRDC# is active only when the memory decode is within the low 1MB of memory space. MRDC# is active on all memory read cycles. MRDC# may be driven by any microprocessor or DMA controller in the system. SMRDC is derived from MRDC# and the decode of the low 1MB of memory. When a microprocessor on the I/O channel wishes to drive MRDC#, it must have the address lines valid on the bus for one system clock period before driving MRDC# active. Both signals are active low.

SMWTC# (O), MWTC# (I/O)

These signals instruct the memory devices to store the data present on the data bus. SMWTC# is active only when the memory decode is within the low 1MB of the memory space. MWTC# is active on all memory write cycles. MWTC# may be driven by any microprocessor or DMA controller in the system. SMWTC# is derived from MWTC# and the decode of the low 1MB of memory. When a microprocessor on the I/O channel wishes to drive MWTC#, it must have the address lines valid on the bus for one system clock period before driving MWTC# active. Both signals are active low.

T-C (O)

Terminal Count (T-C) provides a pulse when the terminal count for any DMA channel is reached.

I/O ADDRESS MAP*

Hex Range	Device
000-01F	DMA Controller 1
020-03F	Interrupt Controller 1, Master
040-05F	Timer
060-06F	8042 (Keyboard)
070-07F	Real-time Clock, NMI (non-maskable interrupt) Mask
080-09F	DMA Page Register
0A0-0BF	Interrupt Controller 2
0C0-0DF	DMA Controller 2
0F0	Clear Math Coprocessor Busy
0F1	Reset Math Coprocessor
0F8-0FF	Math Coprocessor
1F0-1F8	Fixed Disk
200-207	Game I/O
278-27F	Parallel Printer Port 2
2F8-2FF	Serial Port 2
300-31F	Prototype Card
360-36F	Reserved
378-37F	Parallel Printer Port 1
380-38F	SDLC, Bisynchronous 2
3A0-3AF	Bisynchronous 1
3B0-3BF	Monochrome Display and Printer Adapter
3C0-3CF	Reserved
3D0-3DF	Color/Graphics Monitor Adapter
3F0-3F7	Diskette Controller
3F8-3FF	Serial Port 1

INTERRUPT ASSIGNMENTS*

Interrupt	Description
IRQ0	Timer Output 0
IRQ1	Keyboard (Output Buffer Full)
IRQ2	Interrupt 8 through 15
IRQ3	Serial Port 2
IRQ4	Serial Port 1
IRQ5	Parallel Port 2
IRQ6	Diskette Controller
IRQ7	Parallel Port 1
IRQ8	Real-time Clock Interrupt
IRQ9	Software Redirected to INT 0AH (IRQ2)
IRQ10	Unassigned
IRQ11	Unassigned
IRQ12	Unassigned
IRQ13	Coprocessor
IRQ14	Fixed Disk Controller
IRQ15	Unassigned

* These are typical parameters, which may not reflect your current system.

PCI LOCAL BUS OVERVIEW

The PCI (Peripheral Component Interconnect) Local Bus is a high performance, 32-bit or 64-bit bus with multiplexed address and data lines. It is intended for use as an interconnect mechanism between highly integrated peripheral controller components, peripheral add-in boards and processor/memory systems.

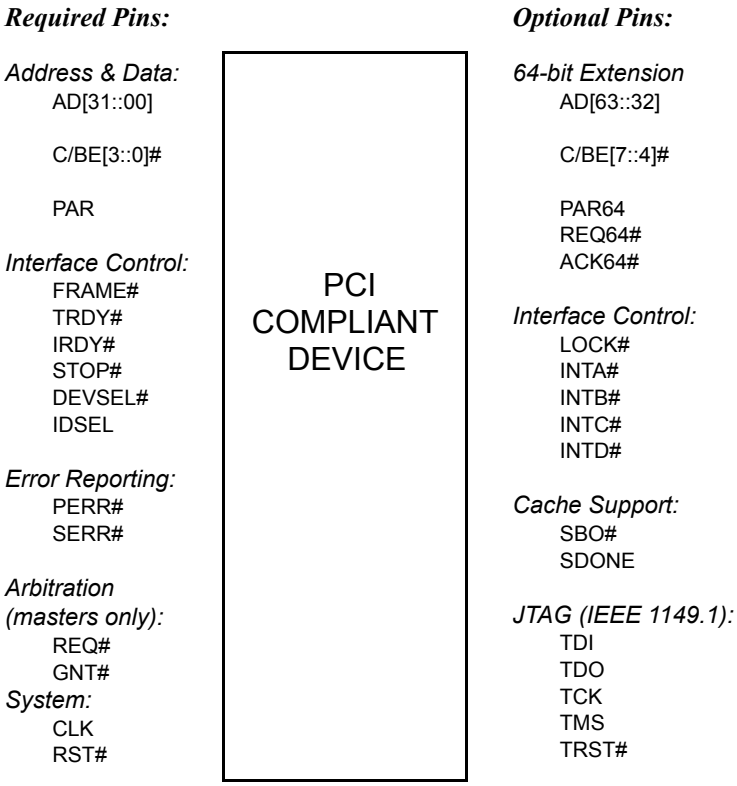
The "local bus" moves peripheral functions with high bandwidth requirements closer to the system's processor bus and can produce substantial performance gains with graphical user interfaces (GUIs) and other high bandwidth functions (i.e., full motion video, SCSI, LANs, etc.).

The PCI Local Bus accommodates future system requirements and is applicable across multiple platforms and architectures.

The PCI component and add-in card interface is processor independent, enabling an efficient transition to future processor generations, by bridges or by direct integration, and use with multiple processor architectures. Processor independence allows the PCI Local Bus to be optimized for I/O functions, enables concurrent operation of the local bus with the processor/memory subsystem, and accommodates multiple high performance peripherals in addition to graphics. Movement to enhanced video and multimedia displays and other high bandwidth I/O will continue to increase local bus bandwidth requirements. A transparent 64-bit extension of the 32-bit data and address buses is defined, doubling the bus bandwidth and offering forward and backward compatibility of 32-bit (132MB/s peak) and 64-bit (264MB/s peak) PCI Local Bus peripherals.

PCI LOCAL BUS SIGNAL DEFINITION

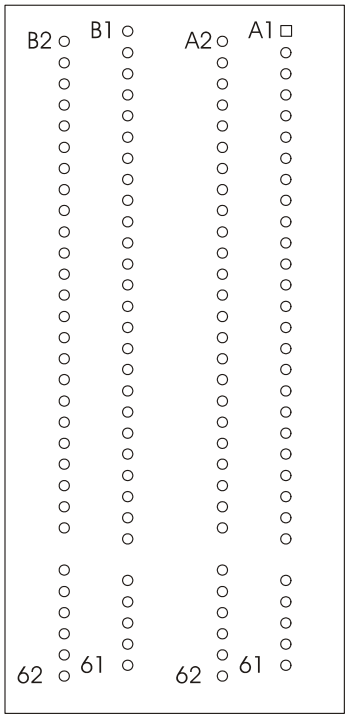
The PCI interface requires a minimum of 47 pins for a target-only device and 49 pins for a master to handle data and addressing, interface control, arbitration and system functions. The diagram below shows the pins in functional groups, with required pins on the left side and optional pins on the right side.



PCI Pin List

PCI LOCAL BUS
PIN NUMBERING

Component Side of Board



5-volt/32-bit PCI Connector

PCI LOCAL BUS PIN ASSIGNMENTS

The PCI Local Bus pin assignments shown below are for the PCI option slots on the backplane.

The PCI Local Bus specifies both 5-volt and 3.3-volt signaling environments. The following bus pin assignments are for the 5-volt connector. The 3.3-volt connector bus pin assignments are the same with the following exceptions:

* The pins noted as +V (I/O) are +5 volts or +3.3 volts, depending on which connector is being used.

† Pins B12, B13, A12 and A13 are Gnd (ground) on the 5-volt connector, but are Connector Keys on the 3.3-volt connector.

†† Pin B49 is Gnd (ground) on the 5-volt connector, but is M66EN on the 3.3-volt connector.

††† Pins B50, B51, A50 and A51 are Connectors Keys on the 5-volt connector, but are Gnd (ground) on the 3.3-volt connector.

I/O Pin	Signal Name	I/O Pin	Signal Name	
B1	-12V	A1	TRST#	32-bit connector
B2	TCK	A2	+12V	
B3	Gnd	A3	TMS	
B4	TDO	A4	TDI	
B5	+5V	A5	+5V	
B6	+5V	A6	INTA#	
B7	INTB#	A7	INTC#	
B8	INTD#	A8	+5V	
B9	PRSNT1#	A9	Reserved	
B10	Reserved	A10	+V (I/O) *	
B11	PRSNT2#	A11	Reserved	
B12	Gnd †	A12	Gnd †	
B13	Gnd †	A13	Gnd †	
B14	Reserved	A14	Reserved	
B15	Gnd	A15	RST#	
B16	CLK	A16	+V (I/O) *	
B17	Gnd	A17	GNT#	
B18	REQ#	A18	Gnd	
B19	+V (I/O) *	A19	Reserved	
B20	AD31	A20	AD30	
B21	AD29	A21	+3.3V	
B22	Gnd	A22	AD28	
B23	AD27	A23	AD26	
B24	AD25	A24	Gnd	
B25	+3.3V	A25	AD24	
B26	C/BE3#	A26	IDSEL	
B27	AD23	A27	+3.3V	
B28	Gnd	A28	AD22	
B29	AD21	A29	AD20	
B30	AD19	A30	Gnd	
B31	+3.3V	A31	AD18	
B32	AD17	A32	AD16	
B33	C/BE2#	A33	+3.3V	
B34	Gnd	A34	FRAME#	
B35	IRDY#	A35	Gnd	

PCI LOCAL BUS PIN ASSIGNMENTS (CONTINUED)

I/O Pin	Signal Name	I/O Pin	Signal Name	
B36	+3.3V	A36	TRDY#	
B37	DEVSEL#	A37	Gnd	
B38	Gnd	A38	STOP#	
B39	LOCK#	A39	+3.3V	
B40	PERR#	A40	SDONE	
B41	+3.3V	A41	SBO#	
B42	SERR#	A42	Gnd	
B43	+3.3V	A43	PAR	
B44	C/BE1#	A44	AD15	
B45	AD14	A45	+3.3V	
B46	Gnd	A46	AD13	
B47	AD12	A47	AD11	
B48	AD10	A48	Gnd	
B49	Gnd ††	A49	AD9	
B50	Connector Key †††	A50	Connector Key †††	5-volt key
B51	Connector Key †††	A51	Connector Key †††	5-volt key
B52	AD8	A52	C/BE0#	
B53	AD7	A53	+3.3V	
B54	+3.3V	A54	AD6	
B55	AD5	A55	AD4	
B56	AD3	A56	Gnd	
B57	Gnd	A57	AD2	
B58	AD1	A58	AD0	
B59	+V (I/O) *	A59	+V (I/O) *	
B60	ACK64#	A60	REQ64#	
B61	+5V	A61	+5V	
B62	+5V	A62	+5V	32-bit connector end

PCI LOCAL BUS PIN ASSIGNMENTS (CONTINUED)

The following pin assignments apply only to backplanes with 64-bit PCI option slots.

I/O Pin	Signal Name	I/O Pin	Signal Name	
	Connector Key		Connector Key	64-bit spacer
	Connector Key		Connector Key	64-bit spacer
B63	Reserved	A63	Gnd	64-bit connector start
B64	Gnd	A64	C/BE7#	
B65	C/BE6#	A65	C/BE5#	
B66	C/BE4#	A66	+V (I/O) *	
B67	Gnd	A67	PAR64	
B68	AD63	A68	AD62	
B69	AD61	A69	Gnd	
B70	+V (I/O) *	A70	AD60	
B71	AD59	A71	AD58	
B72	AD57	A72	Gnd	
B73	Gnd	A73	AD56	
B74	AD55	A74	AD54	
B75	AD53	A75	+V (I/O) *	
B76	Gnd	A76	AD52	
B77	AD51	A77	AD50	
B78	AD49	A78	Gnd	
B79	+V (I/O) *	A79	AD48	
B80	AD47	A80	AD46	
B81	AD45	A81	Gnd	
B82	Gnd	A82	AD44	
B83	AD43	A83	AD42	
B84	AD41	A84	+V (I/O) *	
B85	Gnd	A85	AD40	
B86	AD39	A86	AD38	
B87	AD37	A87	Gnd	
B88	+V (I/O) *	A88	AD36	
B89	AD35	A89	AD34	
B90	AD33	A90	Gnd	
B91	Gnd	A91	AD32	
B92	Reserved	A92	Reserved	
B93	Reserved	A93	Gnd	
B94	Gnd	A94	Reserved	64-bit connector end

PCI LOCAL BUS SIGNAL DESCRIPTIONS

The PCI Local Bus signals are described below and may be categorized into the following functional groups:

- System Pins
- Address and Data Pins
- Interface Control Pins
- Arbitration Pins (Bus Masters Only)
- Error Reporting Pins
- Interrupt Pins (Optional)
- Cache Support Pins (Optional)
- 64-Bit Bus Extension Pins (Optional)
- JTAG/Boundary Scan Pins (Optional)

A # symbol at the end of a signal name indicates that the active state occurs when the signal is at a low voltage. When the # symbol is absent, the signal is active at a high voltage.

The following are descriptions of the PCI Local Bus signals.

ACK64# (optional)

Acknowledge 64-bit Transfer, when actively driven by the device that has positively decoded its address as the target of the current access, indicates the target is willing to transfer data using 64bits. ACK64# has the same timing as DEVSEL#.

AD[31::00]

Address and Data are multiplexed on the same PCI pins. A bus transaction consists of an address phase followed by one or more data phases. During the address phase, AD[31::00] contain a physical address (32 bits). During data phases, AD[07::00] contain the least significant byte (lsb) and AD[31::24] contain the most significant byte (msb).

AD[63::32] (optional)

Address and Data are multiplexed on the same pins and provide 32additional bits. During an address phase (when using the DAC command and when REQ64# is asserted), the upper 32bits of a 64-bit address are transferred; otherwise, these bits are reserved but are stable and indeterminate. During a data phase, an additional 32bits of data are transferred when REQ64# and ACK64# are both asserted.

C/BE[3::0]#

Bus Command and Byte Enables are multiplexed on the same PCI pins. During the address phase of a transaction, these pins define the bus command; during the data phase they are used as byte enables. The byte enables are valid for the entire data phase and determine which byte lanes carry meaningful data. C/BE0# applies to byte0 (lsb) and C/BE3# applies to byte 3 (msb).

C/BE[7::4]# (optional)

Bus Command and Byte Enables are multiplexed on the same pins. During an address phase (when using the DAC command and when REQ64# is asserted), the actual bus command is transferred on C/BE[7::4]#; otherwise, these bits are reserved and indeterminate. During a data phase, C/BE[7::4]# are byte enables indicating which byte lanes carry meaningful data when REQ64# and ACK64# are both asserted. C/BE4# applies to byte4 and C/BE7# applies to byte7.

CLK

Clock provides timing for all transactions on PCI and is an input to every PCI device.

DEVSEL#

Device Select, when actively driven, indicates that the driving device has decoded its address as the target of the current access. As an input, DEVSEL# indicates whether any device on the bus has been selected.

FRAME#

Cycle Frame is an interface control pin which is driven by the current master to indicate the beginning and duration of an access. When FRAME# is asserted, data transfers continue; when it is deasserted, the transaction is in the final data phase.

GNT#

Grant indicates to the agent that access to the bus has been granted. This is a point to point signal. Every master has its own GNT#.

IDSEL

Initialization Device Select is used as a chip select during configuration read and write transactions.

INTA#, INTB#, INTC#, INTD# (optional)

Interrupts on PCI are optional and defined as "level sensitive," asserted low (negative true), using open drain output drivers. PCI defines one interrupt for a single function and up to four interrupt lines for a multi-function device or connector.

Interrupt A is used to request an interrupt. For a single function device, only INTA# may be used, while the other three interrupt lines have no meaning.

Interrupt B, Interrupt C and Interrupt D are used to request additional interrupts and only have meaning on a multi-function device.

IRDY#

Initiator Ready indicates the initiating agent's (bus master's) ability to complete the current data phase of the transaction. IRDY# is used in conjunction with TRDY#. During a write, IRDY# indicates that valid data is present on AD[31::0]. During a read, it indicates that the master is prepared to accept data.

LOCK#

Lock indicates an operation that may require multiple transactions to complete. When LOCK# is asserted, non-exclusive transactions may proceed to an address that is not currently locked.

PAR

Parity is even parity across AD[31::00] and C/BE[3::0]#. Parity generation is required by all PCI agents. The master drives PAR for address and write data phases; the target drives PAR for read data phases.

PAR64 (optional)

Parity Upper DWORD is the even parity bit that protects AD[63::32] and C/BE[7::4]#. The master drives PAR64 for address and write data phases; the target drives PAR64 for read data phases.

PERR#

Parity Error is for the reporting of data parity errors during all PCI transactions except a Special Cycle. There are no special conditions when a data parity error may be lost or when reporting of an error may be delayed.

PRSNT1# and PRSNT2#

PRSNT1# and PRSNT2# are related to the connector only, not to other PCI components. They are used for two purposes: indicating that a board is physically present in the slot and providing information about the total power requirements of the board.

REQ#

Request indicates to the arbiter that this agent desires use of the bus. This is a point to point signal. Every master has its own REQ#.

REQ64# (optional)

Request 64-bit Transfer, when actively driven by the current bus master, indicates it desires to transfer data using 64 bits. REQ64# has the same timing as FRAME#. REQ64# has meaning at the end of reset.

RST#

Reset is used to bring PCI-specific registers, sequencers and signals to a consistent state.

SBO# (optional)

Snoop Backoff is an optional cache support pin which indicates a hit to a modified line when asserted. When SBO# is deasserted and SDONE is asserted, it indicates a "clean" snoop result.

SDONE (optional)

Snoop Done is an optional cache support pin which indicates the status of the snoop for the current access. When deasserted, it indicates the result of the snoop is still pending. When asserted, it indicates the snoop is complete.

SERR#

System Error is for reporting address parity errors, data parity errors on the Special Cycle command, or any other system error where the result will be catastrophic. If an agent does not want a non-maskable interrupt (NMI) to be generated, a different reporting mechanism is required.

STOP#

Stop indicates that the current target is requesting the master to stop the current transaction.

TCK (optional)

Test Clock is used to clock state information and test data into and out of the device during operation of the TAP (Test Access Port).

TDI (optional)

Test Data Input is used to serially shift test data and test instructions into the device during TAP (Test Access Port) operation.

TDO (optional)

Test Data Output is used to serially shift test data and test instructions out of the device during TAP (Test Access Port) operation.

TMS (optional)

Test Mode Select is used to control the state of the TAP (Test Access Port) controller in the device.

TRDY#

Target Ready indicates the target agent's (selected device's) ability to complete the current data phase of the transaction. TRDY# is used in conjunction with IRDY#. During a read, TRDY# indicates that valid data is present on AD[31::00]. During a write, it indicates that the target is prepared to accept data.

TRST# (optional)

Test Reset provides an asynchronous initialization of the TAP controller. This signal is optional in the IEEE Standard Test Access Port and Boundary Scan Architecture.

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Chapter 3 PCI/ISA Backplanes

5457-000
BP3/16

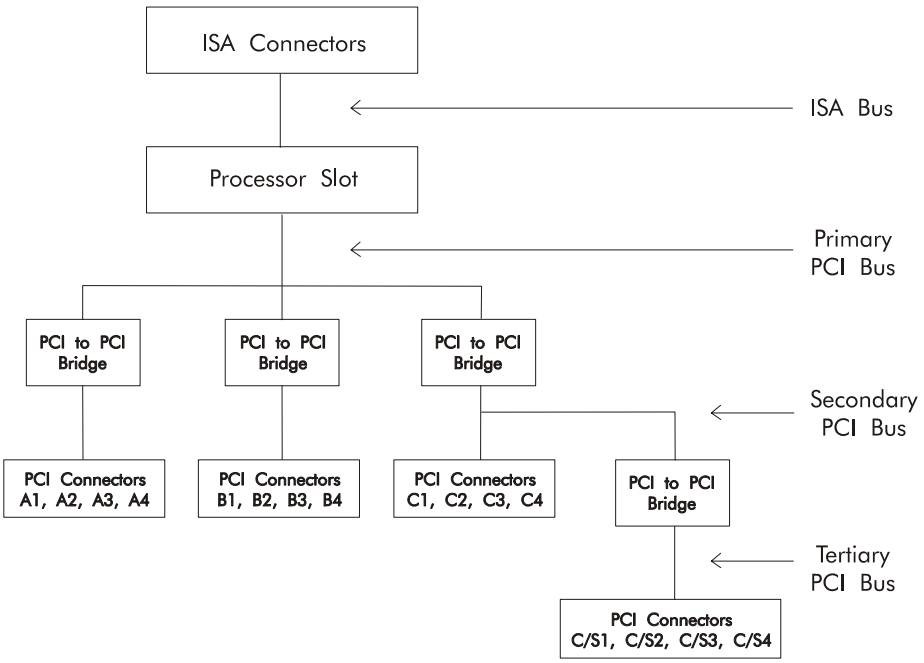
The BP3/16 is a PICMG-compatible backplane. It is a six-layer .062" thick PCB which provides three ISA slots and 16 PCI Local Bus slots for use by standard PCI Local Bus option cards.

One of the three ISA slots is dedicated to the SBC with PCI extension. The PCI slots support the PCI Local Bus 2.1 Specification. Of the 16 PCI slots, 12 slots are on the secondary PCI Bus, which is implemented using three Intel PCI-to-PCI bridges. The remaining four PCI slots are on the tertiary PCI Bus, which is implemented using a fourth Intel PCI-to-PCI bridge.

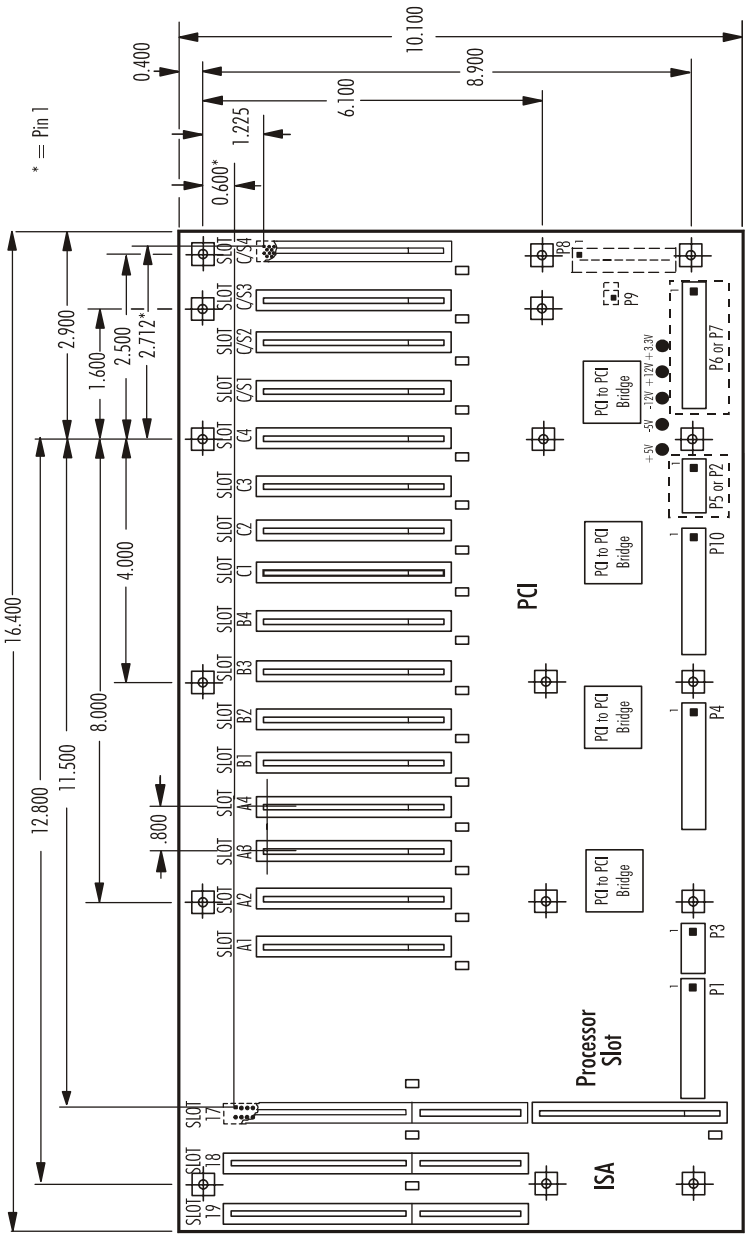
The standard AT power connection is available through two 12-pin .156 MTA connectors or one terminal block connector. Power connection for +3.3V is available through a 12-pin .156 MTA connector or an ATX connector (optional).

An extended-current option is also available. The extended-current connectors provide additional power capacity up to 150 Amps of +5V for power-intensive applications.

5457-000
BP3/16
BUS DIAGRAM



5457-000
BP3/16
DIMENSIONAL
DRAWING



PCB thickness .062”
Mounting holes .156” diameter
Connector spacing .800” centers

5457-000
BP3/16
CONNECTORS

NOTE: Pin 1 on the connectors is indicated by the square pad on the PCB.

P1 - Power Supply Connector
12 pin right angle, Molex #26-60-5120

Pin	Signal
1	NC
2	+5V
3	+12V
4	-12V
5	Gnd
6	Gnd
7	Gnd
8	Gnd
9	-5V
10	+5V
11	+5V
12	+5V

P2 - +5V Extended-Current Connector (optional)
5 pin right angle, Amp #193839-4
31 Amps per circuit
(Refer to Amp Doc. #108-1594)

Pin	Signal
1	+5V
2	+5V
3	+5V
4	+5V
5	+5V

P3 - Auxiliary Power Supply Connector
6 pin right angle, Molex #26-60-5060

Pin	Signal
1	+5V
2	+5V
3	+5V
4	Gnd
5	Gnd
6	Gnd

5457-000
BP3/16
CONNECTORS (CONTINUED)

P4 - Alternate Power Supply Connector
10 position terminal block, Augat #2MV-10
20 Amps per circuit

Pin	Signal
1	+5V
2	+5V
3	+5V
4	Gnd
5	Gnd
6	Gnd
7	Gnd
8	-5V
9	-12V
10	+12V

P5 - Auxiliary Power Supply Connector
6 pin right angle, Molex #26-60-5060

Pin	Signal
1	+5V
2	+5V
3	+5V
4	Gnd
5	Gnd
6	Gnd

P6 - Power Supply Connector
12 pin right angle, Molex #26-60-5120

Pin	Signal
1	NC
2	+5V
3	+12V
4	-12V
5	Gnd
6	Gnd
7	Gnd
8	Gnd
9	-5V
10	+5V
11	+5V
12	+5V

5457-000
BP3/16
CONNECTORS (CONTINUED)

P7 - +5V Return Extended-Current Connector (optional)
5 pin right angle, Amp #193839-4
31 Amps per circuit
(Refer to Amp Doc. #108-1594)

Pin	Signal
1	Gnd
2	Gnd
3	Gnd
4	Gnd
5	Gnd

P8 - ATX Connector (optional)
20 pin dual row header, Molex #39-29-9202

Pin	Signal	Pin	Signal
1	+3.3V	11	+3.3V
2	+3.3V	12	-12V
3	Gnd	13	Gnd
4	+5V	14	PS-ON
5	Gnd	15	Gnd
6	+5V	16	Gnd
7	Gnd	17	Gnd
8	PW-OK	18	-5V
9	+5VSB	19	+5V
10	+12V	20	+5V

P9 - ATX Power-On Connector (optional)
2 pin header, Amp #640456-2

Pin	Signal
1	PS-ON
2	Gnd

P10 - +3.3V Power Supply Connector
12 pin right angle, Molex #26-60-5120

Pin	Signal
1	+3.3V
2	+3.3V
3	+3.3V
4	Gnd
5	Gnd
6	Gnd
7	Gnd
8	Gnd
9	Gnd
10	+3.3V
11	+3.3V
12	+3.3V

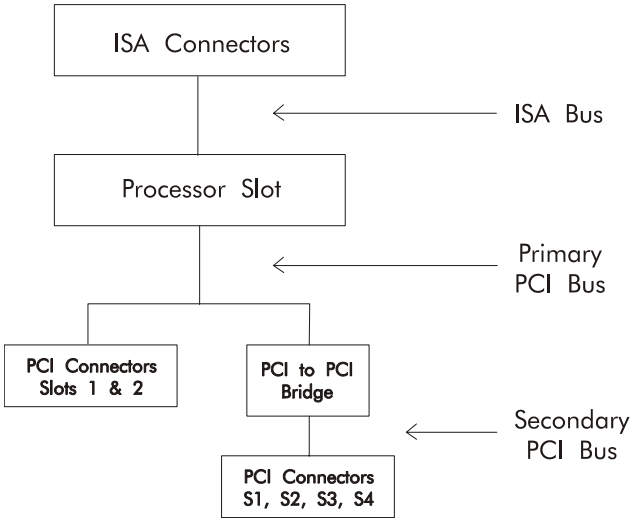
5491-000
BP7/6

The BP7/6 is a PICMG-compatible backplane. It is a six-layer .062" thick PCB which provides seven ISA slots and six PCI Local Bus slots for use by standard PCI Local Bus option cards.

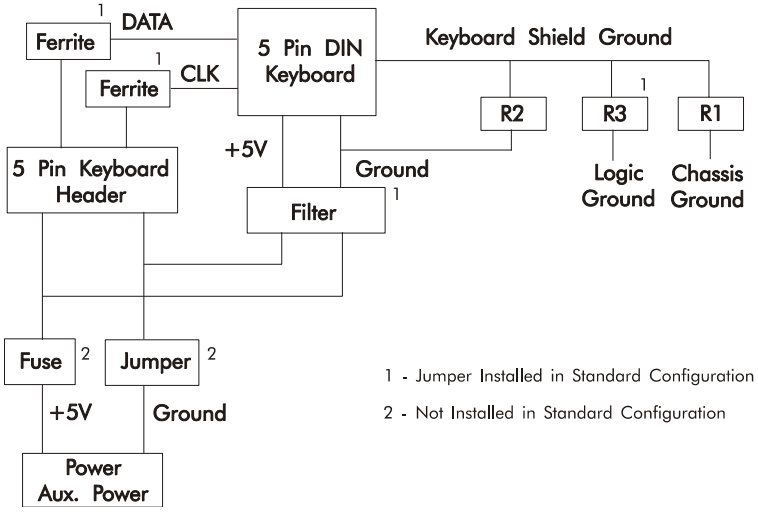
One of the seven ISA slots is dedicated to the SBC with PCI extension. The PCI slots support the PCI Local Bus 2.1 Specification. Two PCI slots are on the primary PCI Bus and four slots are on the secondary PCI Bus. The secondary PCI Bus is implemented using an Intel PCI-to-PCI bridge.

The standard AT power connection is available through a 12-pin AT-style connector. Power connection for +3.3V is available through a 12-pin AT-style connector or an ATX connector (optional).

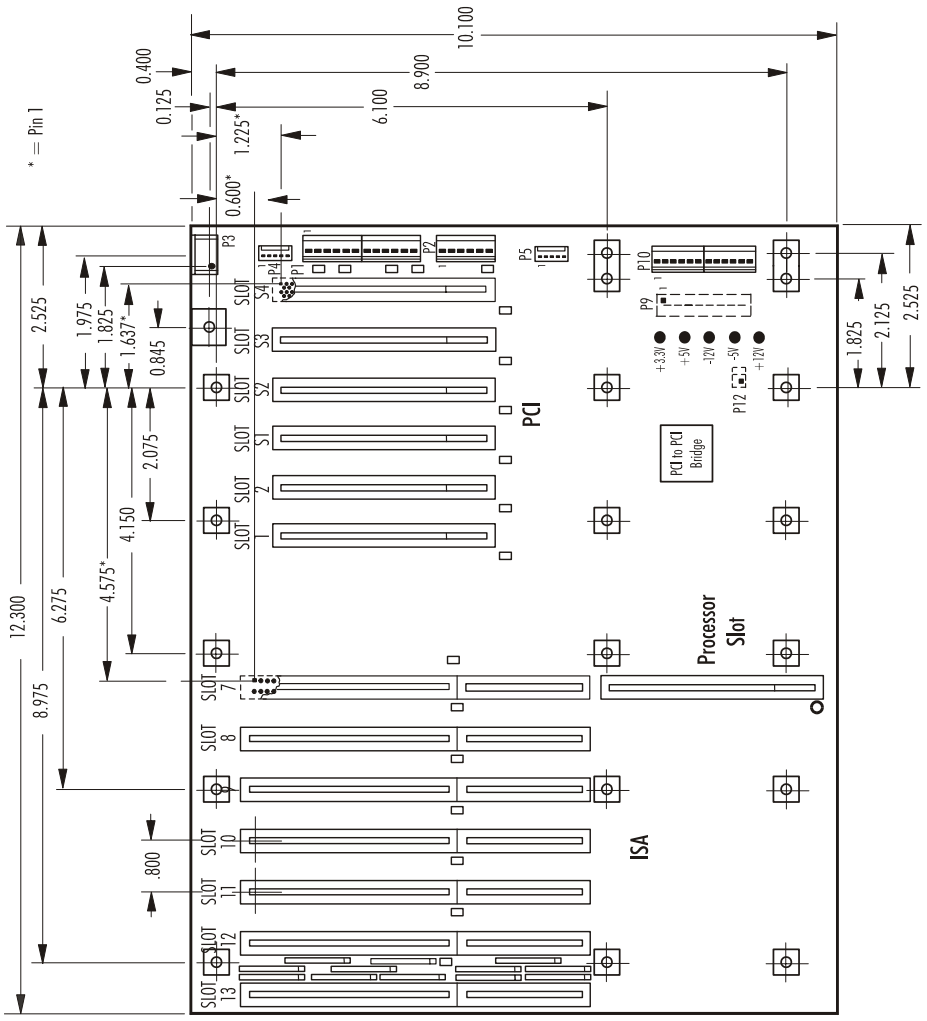
5491-000
BP7/6
BUS DIAGRAM



KEYBOARD
DIAGRAM



5491-000
BP7/6
DIMENSIONAL DRAWING



PCB thickness .062”
Mounting holes .156” diameter
Connector spacing .800” centers

5491-000
BP7/6
CONNECTORS

NOTE: Pin 1 on the connectors is indicated by the square pad on the PCB.

P1 - Power Supply Connector
12 pin single row header, Leoco #4301P12V000

Pin	Signal
1	NC
2	+5V
3	+12V
4	-12V
5	Gnd
6	Gnd
7	Gnd
8	Gnd
9	-5V
10	+5V
11	+5V
12	+5V

P2 - Auxiliary Power Supply Connector
6 pin single row header, Burndy #GTC6R-1

Pin	Signal
1	+5V
2	+5V
3	+5V
4	Gnd
5	Gnd
6	Gnd

P3 - Keyboard Connector
5 pin DIN, Amp #520842-1

Pin	Signal
1	Kbd Clock
2	Kbd Data
3	NC
4	Kbd Gnd
5	Kbd Power (+5V fused)

5491-000
BP7/6
CONNECTORS (CONTINUED)

P4 - Keyboard Connector
5 pin single row header, Amp #640456-5

Pin	Signal
1	Kbd Clock
2	Kbd Data
3	NC
4	Kbd Gnd
5	Kbd Power (+5V fused)

P5 - Keyboard Connector
5 pin single row header, Amp #640456-5

Pin	Signal
1	Kbd Clock
2	Kbd Data
3	NC
4	Kbd Gnd
5	Kbd Power (+5V fused)

P9 - ATX Connector (optional)
20 pin dual row header, Molex #39-29-9202

Pin	Signal	Pin	Signal
1	+3.3V	11	+3.3V
2	+3.3V	12	-12V
3	Gnd	13	Gnd
4	+5V	14	PS-ON
5	Gnd	15	Gnd
6	+5V	16	Gnd
7	Gnd	17	Gnd
8	PW-OK	18	-5V
9	+5VSB	19	+5V
10	+12V	20	+5V

P10 - +3.3V Power Supply Connector
12 pin single row header, Leoco #4301P12V000

Pin	Signal
1	+3.3V
2	+3.3V
3	+3.3V
4	Gnd
5	Gnd
6	Gnd
7	Gnd
8	Gnd
9	Gnd

5491-000 BP7/6 CONNECTORS (CONTINUED)

P10 - +3.3V Power Supply Connector (continued)

Pin	Signal
10	+3.3V
11	+3.3V
12	+3.3V

P12 - ATX Power-On Connector (optional)
2 pin header, Amp #640456-2

Pin	Signal
1	PS-ON
2	Gnd

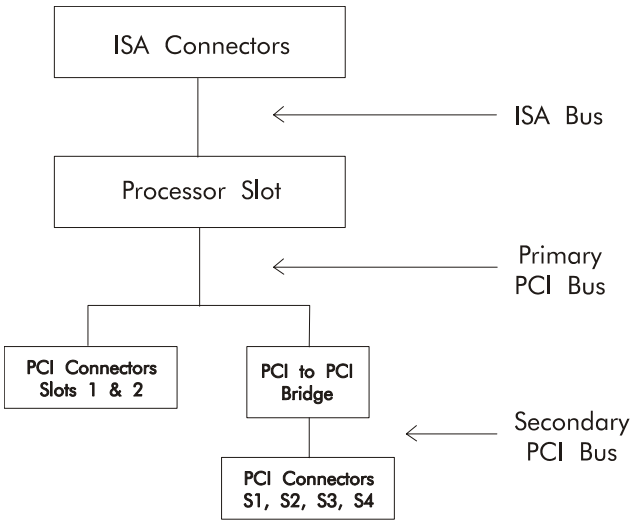
5495-000
BP13/6

The BP13/6 is a PICMG-compatible backplane. It is a six-layer .062" thick PCB which provides 13 ISA slots and six PCI Local Bus slots for use by standard PCI Local Bus option cards.

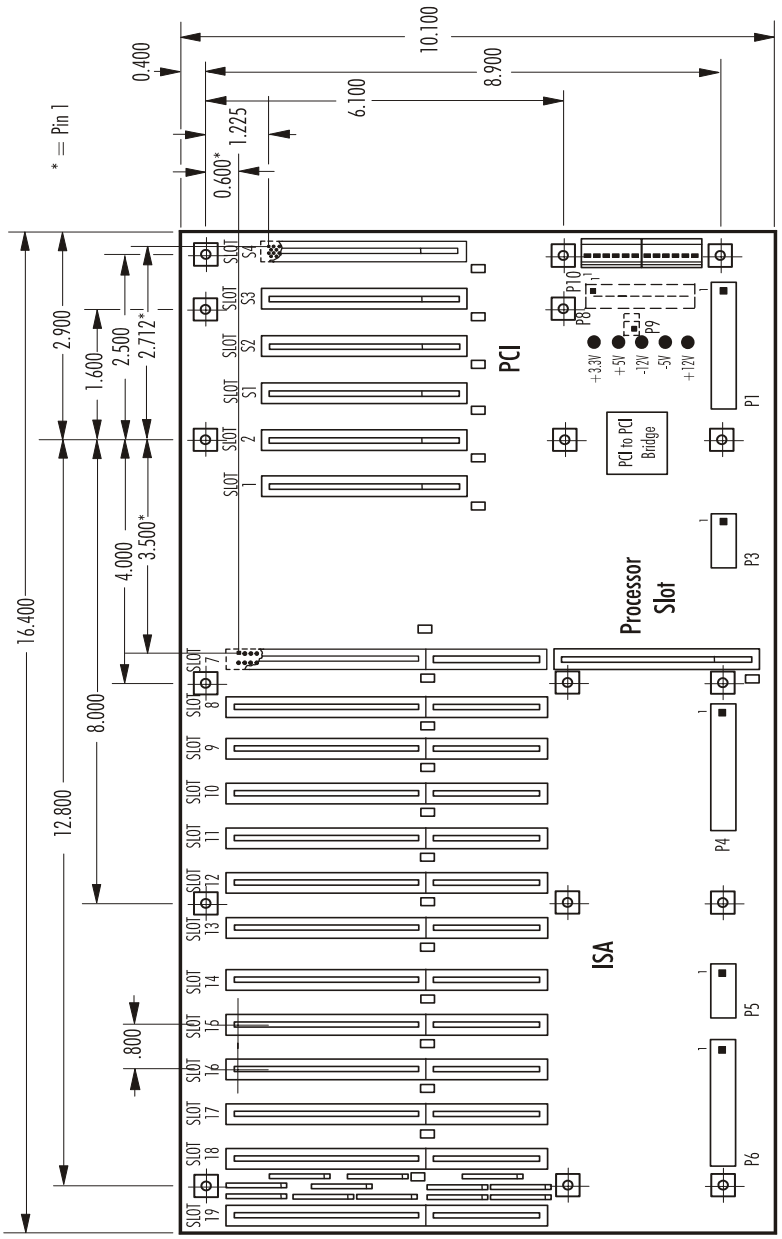
One of the 13 ISA slots is dedicated to the SBC with PCI extension. The PCI slots support the PCI Local Bus 2.1 Specification. Two PCI slots are on the primary PCI Bus and four slots are on the secondary PCI Bus. The secondary PCI Bus is implemented using an Intel PCI-to-PCI bridge.

The standard AT power connection is available through two 12-pin .156 MTA connectors or one terminal block connector. Power connection for +3.3V is available through a 12-pin AT-style connector or an ATX connector (optional).

5495-000
BP13/6
BUS DIAGRAM



5495-000
BP13/6
DIMENSIONAL DRAWING



PCB thickness .062”
Mounting holes .156” diameter
Connector spacing .800” centers

5495-000 BP13/6 CONNECTORS

NOTE: Pin 1 on the connectors is indicated by the square pad on the PCB.

P1 - Power Supply Connector
12 pin right angle, Molex #26-60-5120

Pin	Signal
1	NC
2	+5V
3	+12V
4	-12V
5	Gnd
6	Gnd
7	Gnd
8	Gnd
9	-5V
10	+5V
11	+5V
12	+5V

P3 - Auxiliary Power Supply Connector
6 pin right angle, Molex #26-60-5060

Pin	Signal
1	+5V
2	+5V
3	+5V
4	Gnd
5	Gnd
6	Gnd

P4 - Alternate Power Supply Connector
10 position terminal block, Augat #2MV-10

Pin	Signal
1	+5V
2	+5V
3	+5V
4	Gnd
5	Gnd
6	Gnd
7	Gnd
8	-5V
9	-12V
10	+12V

5495-000
BP13/6
CONNECTORS (CONTINUED)

P5 - Auxiliary Power Supply Connector
6 pin right angle, Molex #26-60-5060

Pin	Signal
1	+5V
2	+5V
3	+5V
4	Gnd
5	Gnd
6	Gnd

P6 - Power Supply Connector
12 pin right angle, Molex #26-60-5120

Pin	Signal
1	NC
2	+5V
3	+12V
4	-12V
5	Gnd
6	Gnd
7	Gnd
8	Gnd
9	-5V
10	+5V
11	+5V
12	+5V

P8 - ATX Connector (optional)
20 pin dual row header, Molex #39-29-9202

Pin	Signal	Pin	Signal
1	+3.3V	11	+3.3V
2	+3.3V	12	-12V
3	Gnd	13	Gnd
4	+5V	14	PS-ON
5	Gnd	15	Gnd
6	+5V	16	Gnd
7	Gnd	17	Gnd
8	PW-OK	18	-5V
9	+5VSB	19	+5V
10	+12V	20	+5V

5495-000 BP13/6 CONNECTORS (CONTINUED)

P9 - ATX Power-On Connector (optional)
2 pin header, Amp #640456-2

Pin	Signal
1	PS-ON
2	Gnd

P10 - +3.3V Power Supply Connector
12 pin single row header, Leoco #4301P12V000

Pin	Signal
1	+3.3V
2	+3.3V
3	+3.3V
4	Gnd
5	Gnd
6	Gnd
7	Gnd
8	Gnd
9	Gnd
10	+3.3V
11	+3.3V
12	+3.3V

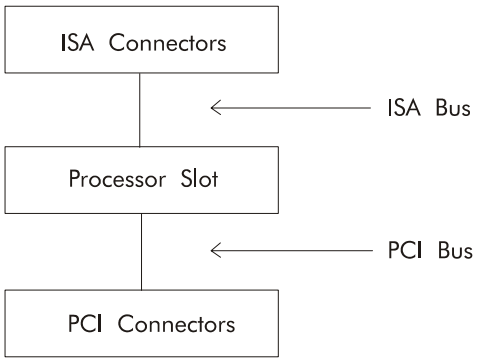
5498-000
BP17/3

The BP17/3 is a PICMG-compatible backplane. It is a six-layer .062" thick PCB which provides 17 ISA slots and three PCI Local Bus slots for use by standard PCI Local Bus option cards.

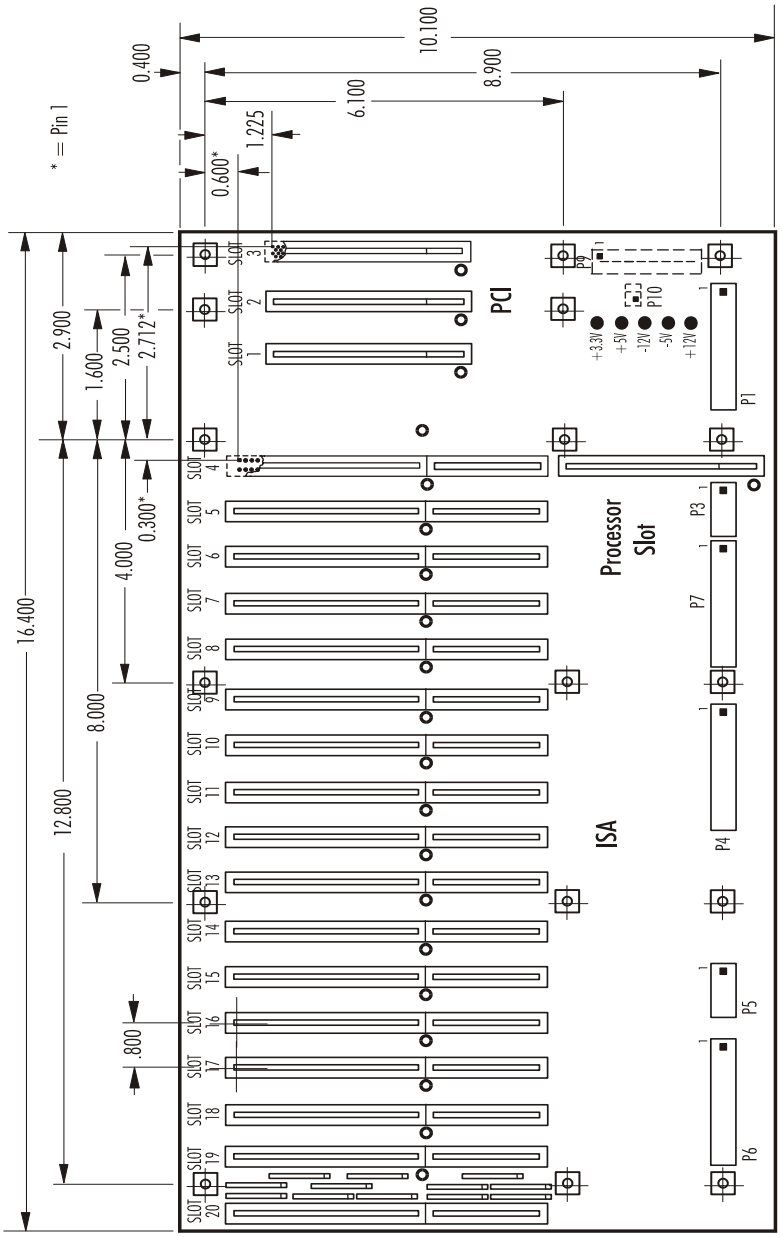
One of the 17 ISA slots is dedicated to the SBC with PCI extension. The PCI slots support the PCI Local Bus 2.1 Specification.

The standard AT power connection is available through two 12-pin .156 MTA connectors or one terminal block connector. Power connection for +3.3V is available through a 12-pin .156 MTA connector or an ATX connector (optional).

5498-000
BP17/3
BUS DIAGRAM



5498-000
BP17/3
DIMENSIONAL DRAWING



PCB thickness .062”
Mounting holes .156” diameter
Connector spacing .800” centers

5498-000
BP17/3
CONNECTORS

NOTE: Pin 1 on the connectors is indicated by the square pad on the PCB.

P1 - Power Supply Connector
12 pin right angle, Molex #26-60-5120

Pin	Signal
1	NC
2	+5V
3	+12V
4	-12V
5	Gnd
6	Gnd
7	Gnd
8	Gnd
9	-5V
10	+5V
11	+5V
12	+5V

P3 - Auxiliary Power Supply Connector
6 pin right angle, Molex #26-60-5060

Pin	Signal
1	+5V
2	+5V
3	+5V
4	Gnd
5	Gnd
6	Gnd

P4 - Alternate Power Supply Connector
10 position terminal block, Augat #2MV-10

Pin	Signal
1	+5V
2	+5V
3	+5V
4	Gnd
5	Gnd
6	Gnd
7	Gnd
8	-5V
9	-12V
10	+12V

5498-000
BP17/3
CONNECTORS (CONTINUED)

P5 - Auxiliary Power Supply Connector
6 pin right angle, Molex #26-60-5060

Pin	Signal
1	+5V
2	+5V
3	+5V
4	Gnd
5	Gnd
6	Gnd

P6 - Power Supply Connector
12 pin right angle, Molex #26-60-5120

Pin	Signal
1	NC
2	+5V
3	+12V
4	-12V
5	Gnd
6	Gnd
7	Gnd
8	Gnd
9	-5V
10	+5V
11	+5V
12	+5V

P7 - +3.3V Power Supply Connector
12 pin right angle, Molex #26-60-5120

Pin	Signal
1	+3.3V
2	+3.3V
3	+3.3V
4	Gnd
5	Gnd
6	Gnd
7	Gnd
8	Gnd
9	Gnd
10	+3.3V
11	+3.3V
12	+3.3V

5498-000
BP17/3
CONNECTORS (CONTINUED)

P9 - ATX Connector (optional)
20 pin dual row header, Molex #39-29-9202

Pin	Signal	Pin	Signal
1	+3.3V	11	+3.3V
2	+3.3V	12	-12V
3	Gnd	13	Gnd
4	+5V	14	PS-ON
5	Gnd	15	Gnd
6	+5V	16	Gnd
7	Gnd	17	Gnd
8	PW-OK	18	-5V
9	+5VSB	19	+5V
10	+12V	20	+5V

P10 - ATX Power-On Connector (optional)
2 pin header, Amp #640456-2

Pin	Signal
1	PS-ON
2	Gnd

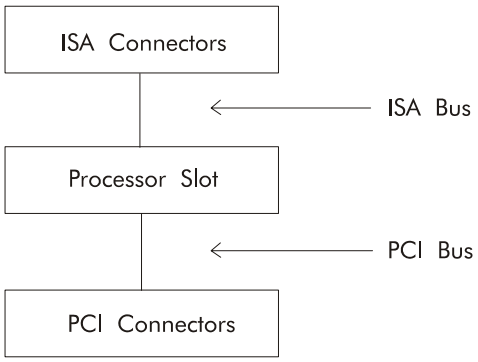
5501-000
BP11/3

The BP11/3 is a PICMG-compatible backplane. It is a six-layer .062" thick PCB which provides 11 ISA slots and three PCI Local Bus slots for use by standard PCI Local Bus option cards.

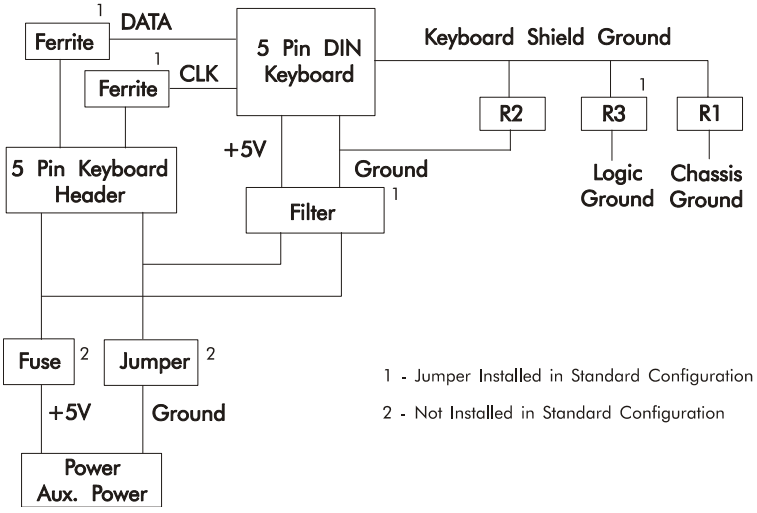
One of the 11 ISA slots is dedicated to the SBC with PCI extension. The PCI slots support the PCI Local Bus 2.1 Specification.

The standard AT power connection is available through a 12-pin AT-style connector. Power connection for +3.3V is available through a 12-pin AT-style connector or an ATX connector (optional).

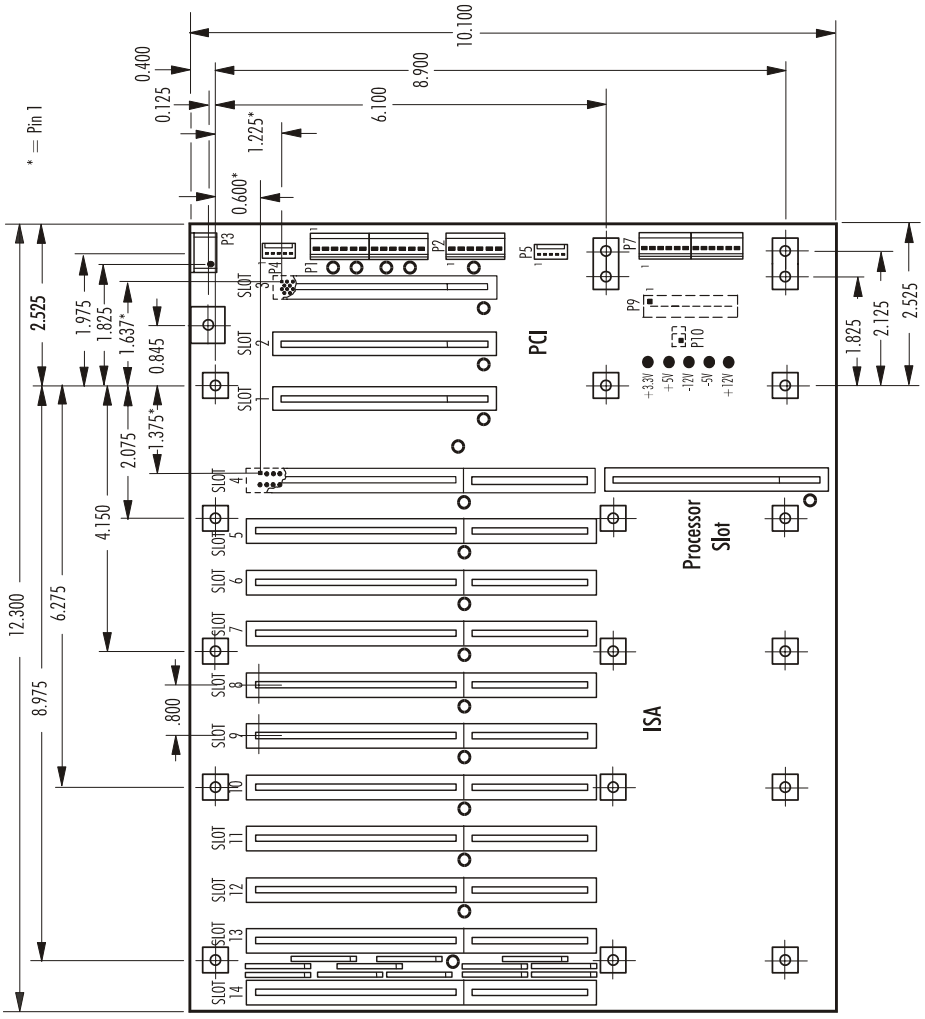
5501-000
BP11/3
BUS DIAGRAM



KEYBOARD DIAGRAM



5501-000
BP11/3
DIMENSIONAL
DRAWING



PCB thickness .062”
Mounting holes .156” diameter
Connector spacing .800” centers

5501-000 BP11/3 CONNECTORS

NOTE: Pin 1 on the connectors is indicated by the square pad on the PCB.

P1 - Power Supply Connector
12 pin single row header, Leoco #4301P12V000

Pin	Signal
1	NC
2	+5V
3	+12V
4	-12V
5	Gnd
6	Gnd
7	Gnd
8	Gnd
9	-5V
10	+5V
11	+5V
12	+5V

P2 - Auxiliary Power Supply Connector
6 pin single row header, Burndy #GTC6R-1

Pin	Signal
1	+5V
2	+5V
3	+5V
4	Gnd
5	Gnd
6	Gnd

P3 - Keyboard Connector
5 pin DIN, Amp #520842-1

Pin	Signal
1	Kbd Clock
2	Kbd Data
3	NC
4	Kbd Gnd
5	Kbd Power (+5V fused)

5501-000
BP11/3
CONNECTORS (CONTINUED)

P4 - Keyboard Connector
5 pin single row header, Amp #640456-5

Pin	Signal
1	Kbd Clock
2	Kbd Data
3	NC
4	Kbd Gnd
5	Kbd Power (+5V fused)

P5 - Keyboard Connector
5 pin single row header, Amp #640456-5

Pin	Signal
1	Kbd Clock
2	Kbd Data
3	NC
4	Kbd Gnd
5	Kbd Power (+5V fused)

P7 - +3.3V Power Supply Connector
12 pin single row header, Leoco #4301P12V000

Pin	Signal
1	+3.3V
2	+3.3V
3	+3.3V
4	Gnd
5	Gnd
6	Gnd
7	Gnd
8	Gnd
9	Gnd
10	+3.3V
11	+3.3V
12	+3.3V

P9 - ATX Connector (optional)
20 pin dual row header, Molex #39-29-9202

Pin	Signal	Pin	Signal
1	+3.3V	11	+3.3V
2	+3.3V	12	-12V
3	Gnd	13	Gnd
4	+5V	14	PS-ON
5	Gnd	15	Gnd
6	+5V	16	Gnd
7	Gnd	17	Gnd

5501-000 BP11/3 CONNECTORS (CONTINUED)

P9 - ATX Connector (continued)

Pin	Signal	Pin	Signal
8	PW-OK	18	-5V
9	+5VSB	19	+5V
10	+12V	20	+5V

P10 - ATX Power-On Connector (optional)
2 pin header, Amp #640456-2

Pin	Signal
1	PS-ON
2	Gnd

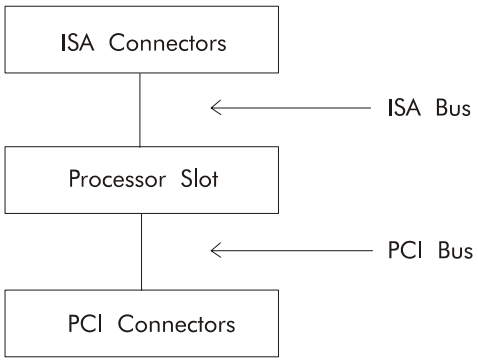
5504-000
BP5/3

The BP5/3 is a PICMG-compatible backplane. It is a six-layer .062" thick PCB which provides five ISA slots and three PCI Local Bus slots for use by standard PCI Local Bus option cards.

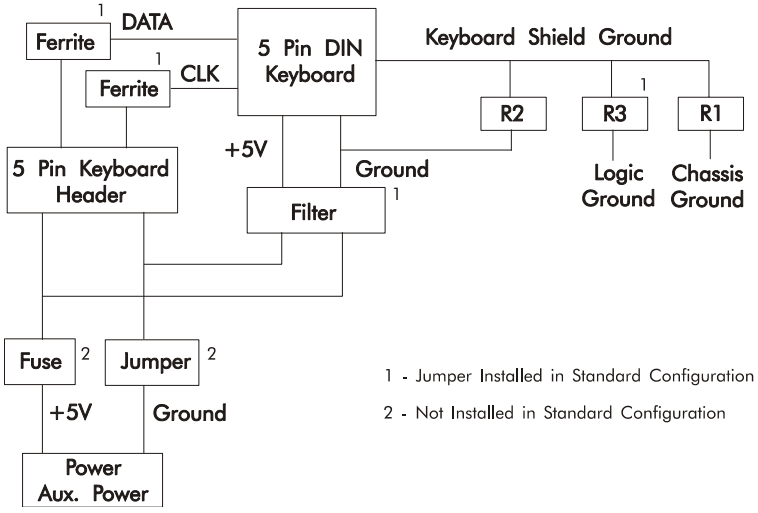
One of the five ISA slots is dedicated to the SBC with PCI extension. The PCI slots support the PCI Local Bus 2.1 Specification.

The standard AT power connection is available through a 12-pin AT-style connector. Power connection for +3.3V is available through a 12-pin AT-style connector or an ATX connector (optional).

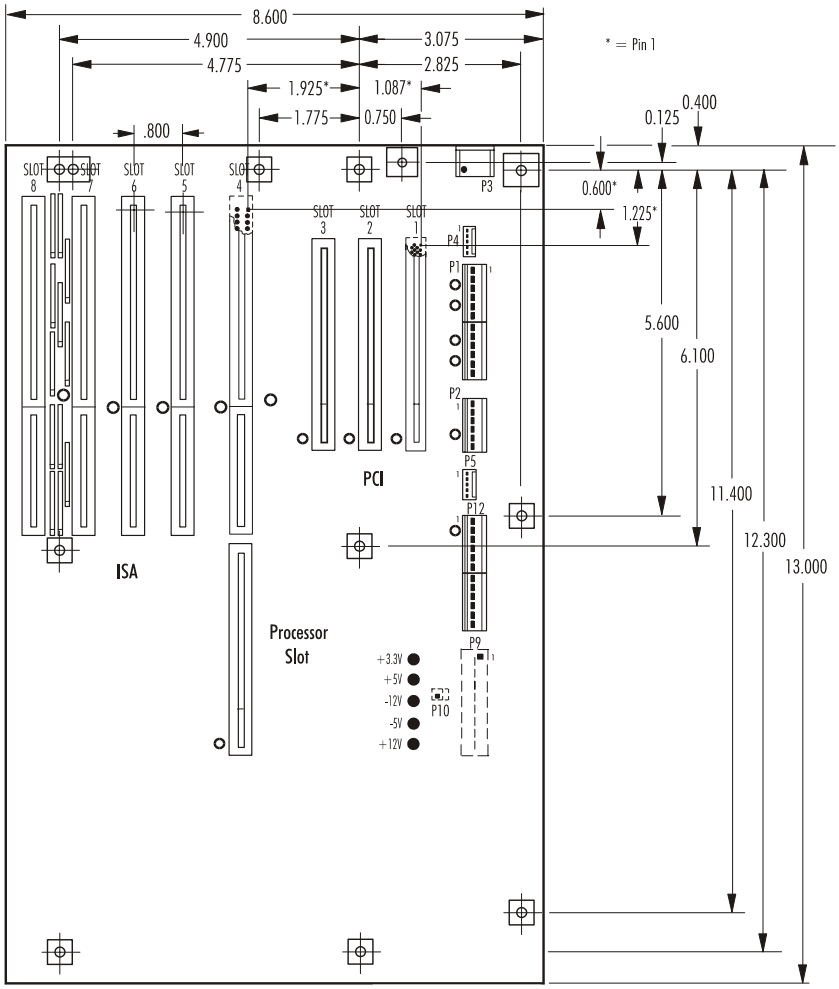
5504-000
BP5/3
BUS DIAGRAM



KEYBOARD DIAGRAM



5504-000
BP5/3
DIMENSIONAL DRAWING



PCB thickness .062”
Mounting holes .156” diameter
Connector spacing .800” centers

5504-000
BP5/3
CONNECTORS

NOTE: Pin 1 on the connectors is indicated by the square pad on the PCB.

P1 - Power Supply Connector
12 pin single row header, Leoco #4301P12V000

Pin	Signal
1	NC
2	+5V
3	+12V
4	-12V
5	Gnd
6	Gnd
7	Gnd
8	Gnd
9	-5V
10	+5V
11	+5V
12	+5V

P2 - Auxiliary Power Supply Connector
6 pin single row header, Burndy #GTC6R-1

Pin	Signal
1	+5V
2	+5V
3	+5V
4	Gnd
5	Gnd
6	Gnd

P3 - Keyboard Connector
5 pin DIN, Amp #520842-1

Pin	Signal
1	Kbd Clock
2	Kbd Data
3	NC
4	Kbd Gnd
5	Kbd Power (+5V fused)

P4 - Keyboard Connector
5 pin single row header, Amp #640456-5

Pin	Signal
1	Kbd Clock
2	Kbd Data
3	NC
4	Kbd Gnd
5	Kbd Power (+5V fused)

5504-000
BP5/3
CONNECTORS (CONTINUED)

P5 - Keyboard Connector
5 pin single row header, Amp #640456-5

Pin	Signal
1	Kbd Clock
2	Kbd Data
3	NC
4	Kbd Gnd
5	Kbd Power (+5V fused)

P9 - ATX Connector (optional)
20 pin dual row header, Molex #39-29-9202

Pin	Signal	Pin	Signal
1	+3.3V	11	+3.3V
2	+3.3V	12	-12V
3	Gnd	13	Gnd
4	+5V	14	PS-ON
5	Gnd	15	Gnd
6	+5V	16	Gnd
7	Gnd	17	Gnd
8	PW-OK	18	-5V
9	+5VSB	19	+5V
10	+12V	20	+5V

P10 - ATX Power-On Connector (optional)
2 pin header, Amp #640456-2

Pin	Signal
1	PS-ON
2	Gnd

P12 - +3.3V Power Supply Connector
12 pin single row header, Leoco #4301P12V000

Pin	Signal
1	+3.3V
2	+3.3V
3	+3.3V
4	Gnd
5	Gnd
6	Gnd
7	Gnd
8	Gnd
9	Gnd
10	+3.3V
11	+3.3V
12	+3.3V

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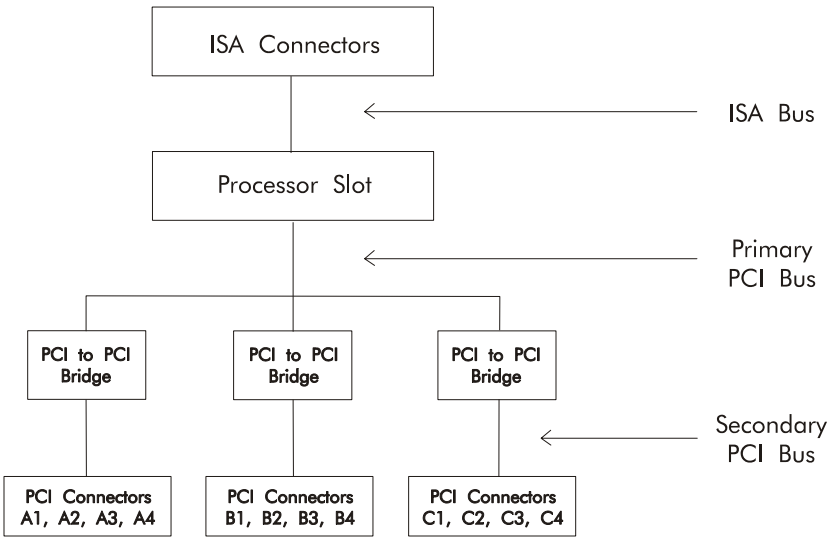
5635-000
BP8/12

The BP8/12 is a PICMG-compatible backplane. It is a six-layer .062" thick PCB which provides eight ISA slots and 12 PCI Local Bus slots for use by standard PCI Local Bus option cards.

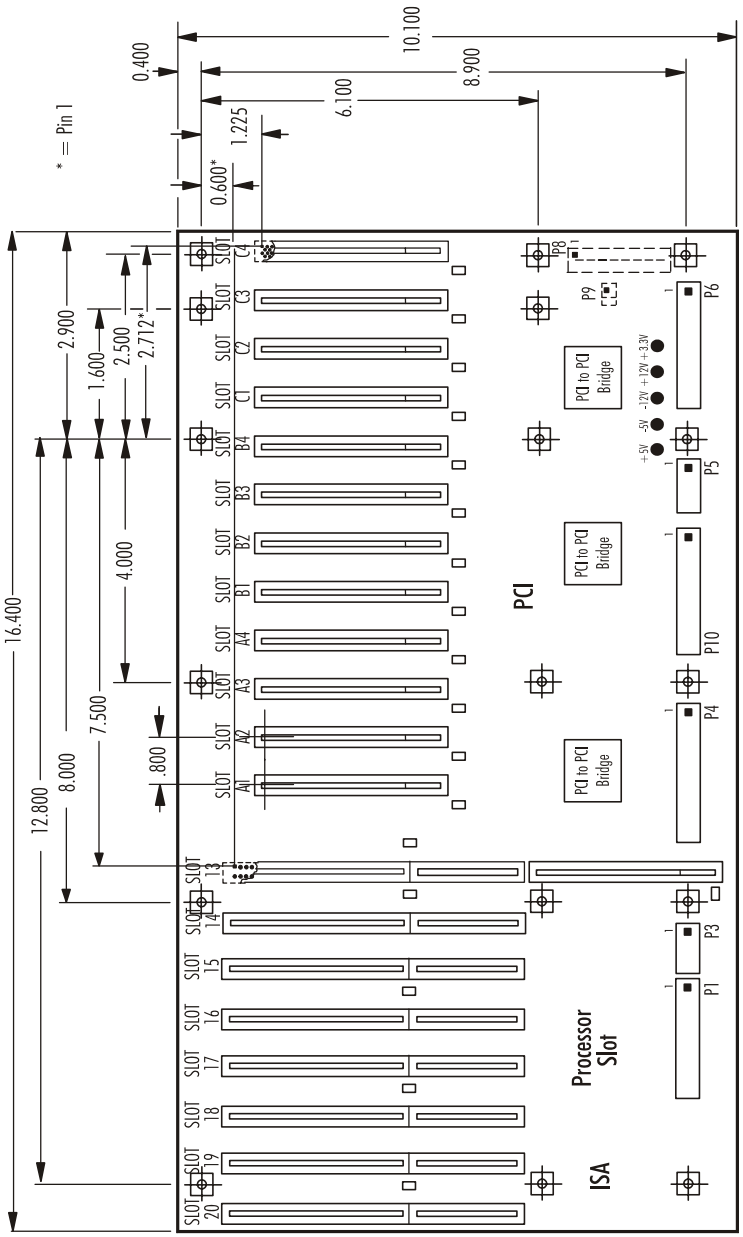
One of the eight ISA slots is dedicated to the SBC with PCI extension. The PCI slots support the PCI Local Bus 2.1 Specification. The 12 PCI slots are on the secondary PCI Bus, which is implemented using three Intel PCI-to-PCI bridges.

The standard AT power connection is available through two 12-pin .156 MTA connectors or one terminal block connector. Power connection for +3.3V is available through a 12-pin .156 MTA connector or an ATX connector (optional).

5635-000
BP8/12
BUS DIAGRAM



5635-000
BP8/12
DIMENSIONAL
DRAWING



PCB thickness .062”
Mounting holes .156” diameter
Connector spacing .800” centers

5635-000
BP8/12
CONNECTORS

NOTE: Pin 1 on the connectors is indicated by the square pad on the PCB.

P1 - Power Supply Connector
12 pin right angle, Molex #26-60-5120

Pin	Signal
1	NC
2	+5V
3	+12V
4	-12V
5	Gnd
6	Gnd
7	Gnd
8	Gnd
9	-5V
10	+5V
11	+5V
12	+5V

P3 - Auxiliary Power Supply Connector
6 pin right angle, Molex #26-60-5060

Pin	Signal
1	+5V
2	+5V
3	+5V
4	Gnd
5	Gnd
6	Gnd

P4 - Alternate Power Supply Connector
12 position terminal block, Augat #2MV-12

Pin	Signal
1	+5V
2	+5V
3	+5V
4	+5V
5	Gnd
6	Gnd
7	Gnd
8	Gnd
9	Gnd
10	-5V
11	-12V
12	+12V

5635-000
BP8/12
CONNECTORS (CONTINUED)

P5 - Auxiliary Power Supply Connector
6 pin right angle, Molex #26-60-5060

Pin	Signal
1	+5V
2	+5V
3	+5V
4	Gnd
5	Gnd
6	Gnd

P6 - Power Supply Connector
12 pin right angle, Molex #26-60-5120

Pin	Signal
1	NC
2	+5V
3	+12V
4	-12V
5	Gnd
6	Gnd
7	Gnd
8	Gnd
9	-5V
10	+5V
11	+5V
12	+5V

P8 - ATX Connector (optional)
20 pin dual row header, Molex #39-29-9202

Pin	Signal	Pin	Signal
1	+3.3V	11	+3.3V
2	+3.3V	12	-12V
3	Gnd	13	Gnd
4	+5V	14	PS-ON
5	Gnd	15	Gnd
6	+5V	16	Gnd
7	Gnd	17	Gnd
8	PW-OK	18	-5V
9	+5VSB	19	+5V
10	+12V	20	+5V

P9 - ATX Power-On Connector (optional)
2 pin header, Amp #640456-2

Pin	Signal
1	PS-ON
2	Gnd

5635-000 BP8/12 CONNECTORS (CONTINUED)

P10 - +3.3V Power Supply Connector
12 pin right angle, Molex #26-60-5120

Pin	Signal
1	+3.3V
2	+3.3V
3	+3.3V
4	Gnd
5	Gnd
6	Gnd
7	Gnd
8	Gnd
9	Gnd
10	+3.3V
11	+3.3V
12	+3.3V

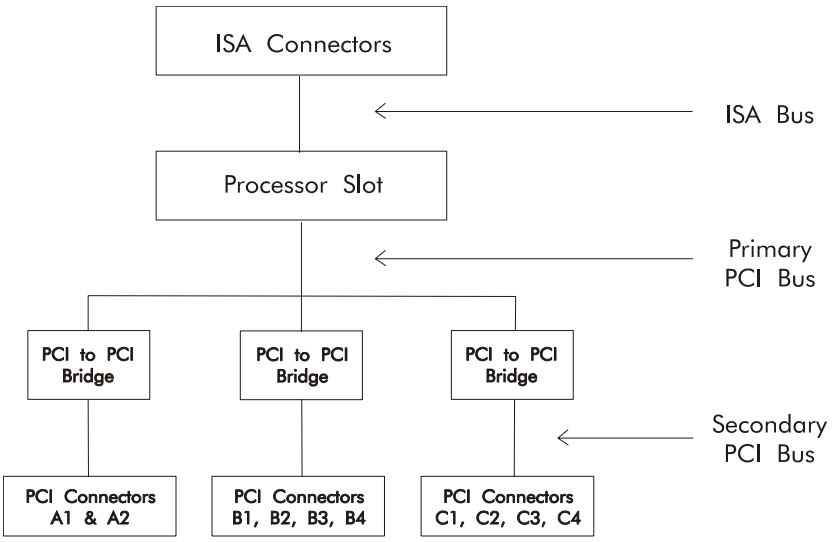
5937-000
BP3/10

The BP3/10 is a PICMG-compatible backplane. It is a six-layer .062" thick PCB which provides three ISA slots and ten 32-bit/33MHz PCI Local Bus slots for use by standard PCI Local Bus option cards.

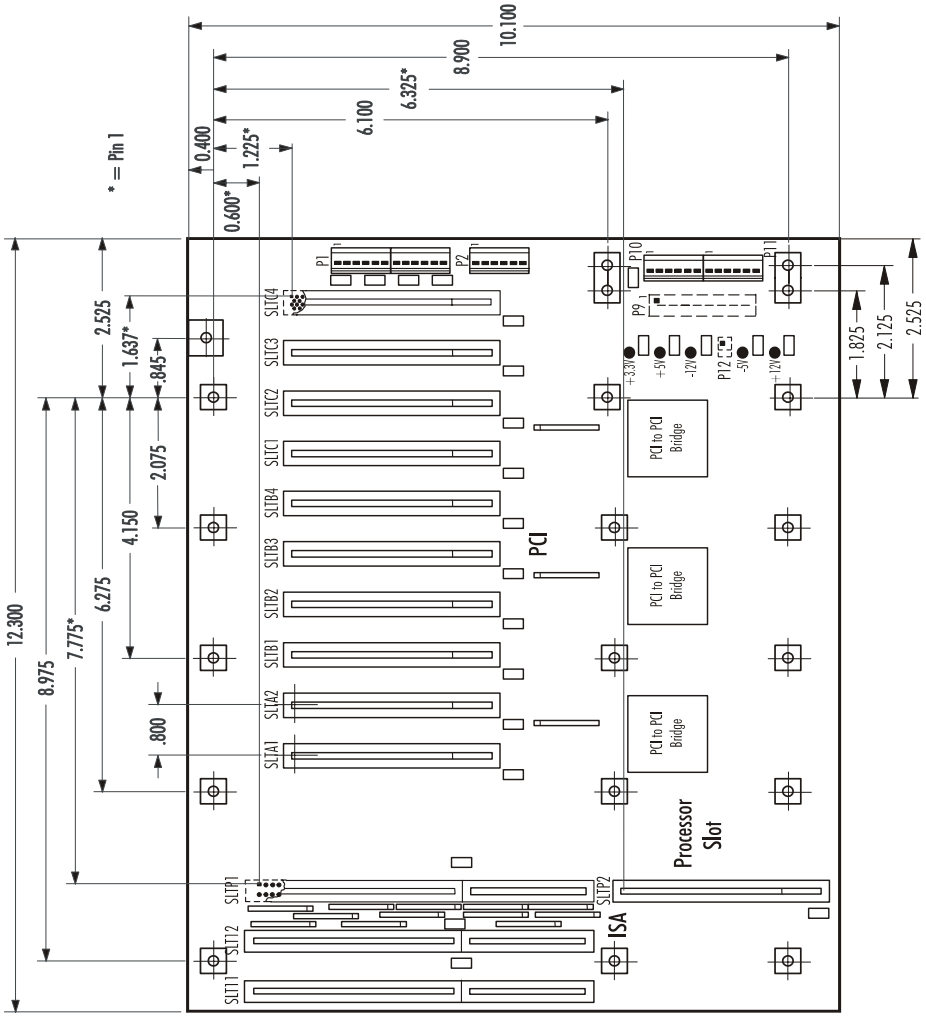
One of the three ISA slots is dedicated to the SBC with PCI extension. The PCI slots support the PCI Local Bus 2.1 Specification. The ten PCI slots are on the secondary PCI Bus, which is implemented using three Intel PCI-to-PCI bridges.

The standard AT power connection is available through a 12-pin AT-style connector. Power connection for +3.3V is available through two 6-pin AT-style connectors or an ATX connector (optional).

5937-000
BP3/10
BUS DIAGRAM



5937-000
BP3/10
DIMENSIONAL DRAWING



PCB thickness .062”
Mounting holes .156” diameter
Connector spacing .800” centers

5937-000
BP3/10
CONNECTORS

NOTE: Pin 1 on the connectors is indicated by the square pad on the PCB.

P1 - Power Supply Connector
12 pin single row header, Leoco #4301P12V000

Pin	Signal
1	NC
2	+5V
3	+12V
4	-12V
5	Gnd
6	Gnd
7	Gnd
8	Gnd
9	-5V
10	+5V
11	+5V
12	+5V

P2 - Auxiliary Power Supply Connector
6 pin single row header, Burndy #GTC6R-1

Pin	Signal
1	+5V
2	+5V
3	+5V
4	Gnd
5	Gnd
6	Gnd

P9 - ATX Connector (optional)
20 pin dual row header, Molex #39-29-9202

Pin	Signal	Pin	Signal
1	+3.3V	11	+3.3V
2	+3.3V	12	-12V
3	Gnd	13	Gnd
4	+5V	14	PS-ON
5	Gnd	15	Gnd
6	+5V	16	Gnd
7	Gnd	17	Gnd
8	PW-OK	18	-5V
9	+5VSB	19	+5V
10	+12V	20	+5V

5937-000
BP3/10
CONNECTORS (CONTINUED)

P10 - +3.3V Power Supply Connector
6 pin single row header, Burndy #GTC6R-1

Pin	Signal
1	+3.3V
2	+3.3V
3	+3.3V
4	Gnd
5	Gnd
6	Gnd

P11 - +3.3V Power Supply Connector
6 pin single row header, Burndy #GTC6R-1

Pin	Signal
1	Gnd
2	Gnd
3	Gnd
4	+3.3V
5	+3.3V
6	+3.3V

P12 - ATX Power-On Connector (optional)
2 pin header, Amp #640456-2

Pin	Signal
1	PS-ON
2	Gnd

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Chapter 4 64-Bit Backplanes

5693-000
BP13/6-64

The BP13/6-64 is a PICMG-compatible backplane. It is a six-layer .062" thick PCB which provides 12 ISA slots, a 64-bit SBC slot and six 64-bit PCI option slots for use by standard PCI Local Bus option cards.

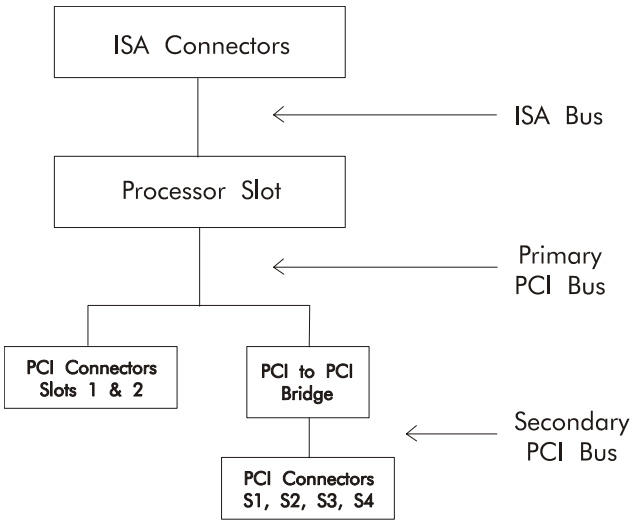
Either 64-bit or 32-bit SBCs and option cards may be used. 64-bit option cards can take advantage of the 64-bit architecture when communicating with each other, even if a 32-bit SBC is used.

The PCI slots support the PCI Local Bus 2.1 Specification. Two of the PCI slots are on the primary PCI Bus and the remaining four PCI slots are on the secondary PCI Bus, which is implemented using an Intel PCI-to-PCI bridge.

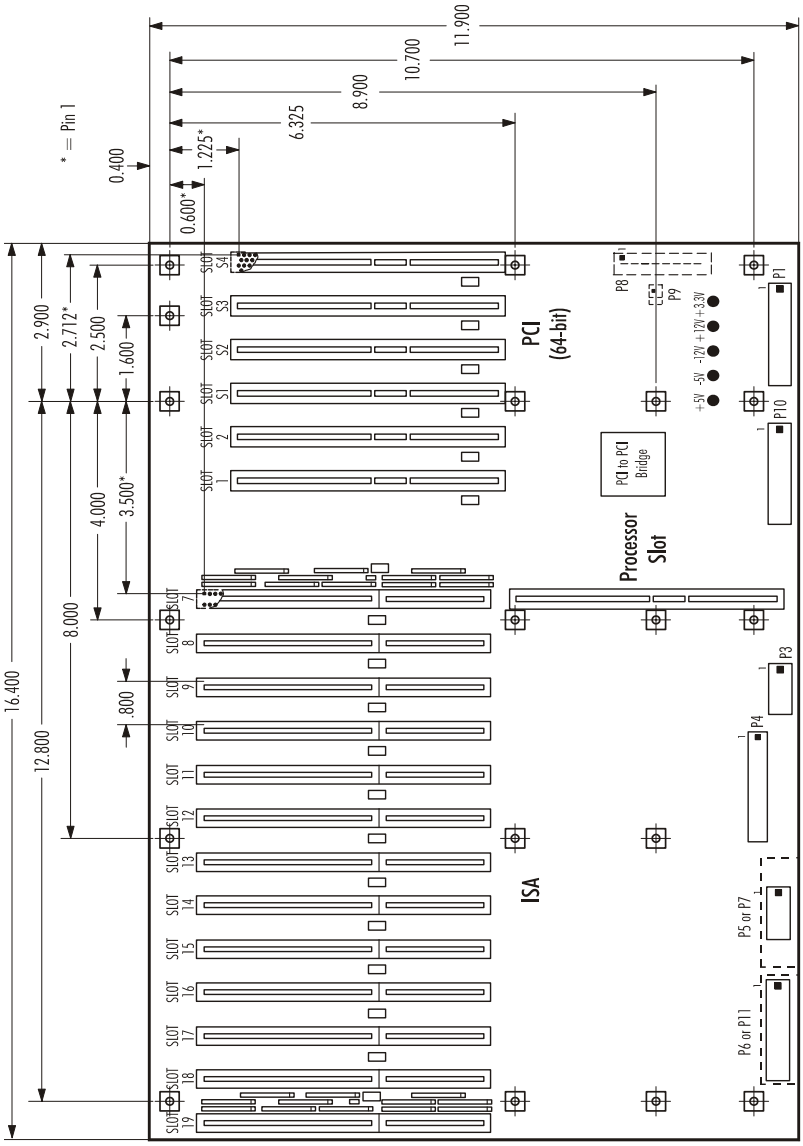
The standard AT power connection is available through two 12-pin .156 MTA connectors or one terminal block connector. Power connection for +3.3V is available through a 12-pin .156 MTA connector or an ATX connector (optional).

An extended-current option is also available. The extended-current connectors provide additional power capacity up to 150 Amps of +5V for power-intensive applications.

5693-000
BP13/6-64
BUS DIAGRAM



5693-000
BP13/6-64
DIMENSIONAL DRAWING



PCB thickness .062”
Mounting holes .156” diameter
Connector spacing .800” centers

5693-000 BP13/6-64 CONNECTORS

NOTE: Pin 1 on the connectors is indicated by the square pad on the PCB.

P1 - Power Supply Connector
12 pin right angle, Molex #26-60-5120

Pin	Signal
1	NC
2	+5V
3	+12V
4	-12V
5	Gnd
6	Gnd
7	Gnd
8	Gnd
9	-5V
10	+5V
11	+5V
12	+5V

P3 - Auxiliary Power Supply Connector
6 pin right angle, Molex #26-60-5060

Pin	Signal
1	+5V
2	+5V
3	+5V
4	Gnd
5	Gnd
6	Gnd

P4 - Alternate Power Supply Connector
10 position terminal block, Augat #2MV-10
20 Amps per circuit

Pin	Signal
1	+5V
2	+5V
3	+5V
4	Gnd
5	Gnd
6	Gnd
7	Gnd
8	-5V
9	-12V
10	+12V

5693-000
BP13/6-64
CONNECTORS (CONTINUED)

P5 - Auxiliary Power Supply Connector
6 pin right angle, Molex #26-60-5060

Pin	Signal
1	+5V
2	+5V
3	+5V
4	Gnd
5	Gnd
6	Gnd

P6 - Power Supply Connector
12 pin right angle, Molex #26-60-5120

Pin	Signal
1	NC
2	+5V
3	+12V
4	-12V
5	Gnd
6	Gnd
7	Gnd
8	Gnd
9	-5V
10	+5V
11	+5V
12	+5V

P7 - +5V Extended-Current Connector (optional)
5 pin right angle, Amp #193839-4
31 Amps per circuit
(Refer to Amp Doc. #108-1594)

Pin	Signal
1	+5V
2	+5V
3	+5V
4	+5V
5	+5V

P8 - ATX Connector (optional)
20 pin dual row header, Molex #39-29-9202

Pin	Signal	Pin	Signal
1	+3.3V	11	+3.3V
2	+3.3V	12	-12V
3	Gnd	13	Gnd
4	+5V	14	PS-ON
5	Gnd	15	Gnd

5693-000
BP13/6-64
CONNECTORS (CONTINUED)

P8 - ATX Connector (continued)

Pin	Signal	Pin	Signal
6	+5V	16	Gnd
7	Gnd	17	Gnd
8	PW-OK	18	-5V
9	+5VSB	19	+5V
10	+12V	20	+5V

P9 - ATX Power-On Connector (optional)
2 pin header, Amp #640456-2

Pin	Signal
1	PS-ON
2	Gnd

P10 - +3.3V Power Supply Connector
12 pin right angle, Molex #26-60-5120

Pin	Signal
1	+3.3V
2	+3.3V
3	+3.3V
4	Gnd
5	Gnd
6	Gnd
7	Gnd
8	Gnd
9	Gnd
10	+3.3V
11	+3.3V
12	+3.3V

P11 - +5V Return Extended-Current Connector (optional)
5 pin right angle, Amp #193839-4
31 Amps per circuit
(Refer to Amp Doc. #108-1594)

Pin	Signal
1	Gnd
2	Gnd
3	Gnd
4	Gnd
5	Gnd

5696-000
BP3/16-64

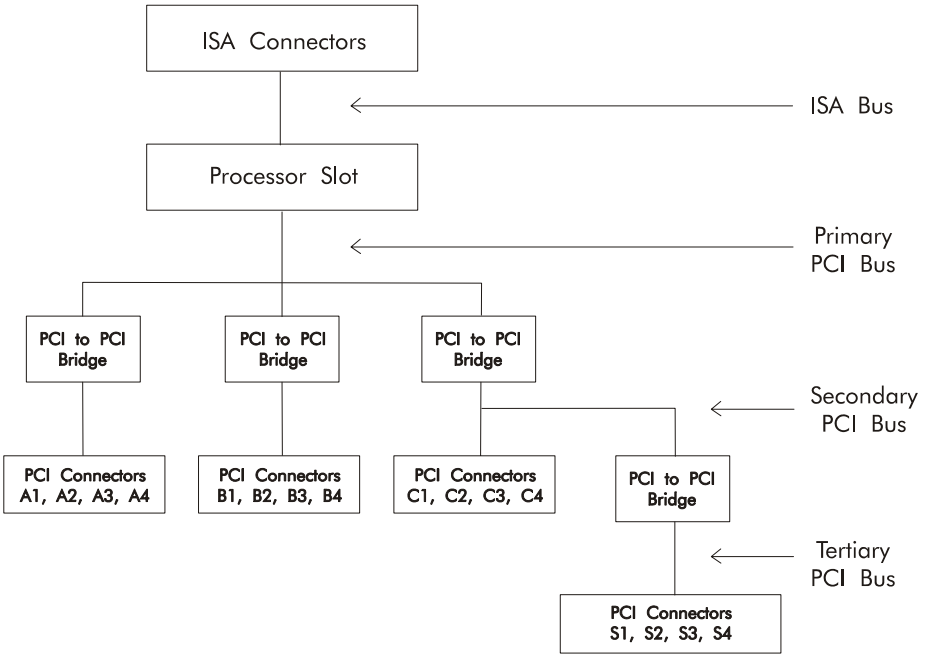
The BP3/16-64 is a PICMG-compatible backplane. It is a six-layer .062" thick PCB which provides two ISA slots, a dedicated SBC slot and 16 64-bit/33MHz PCI Local Bus slots for use by standard PCI Local Bus option cards.

The SBC slot supports SBCs with 32-bit/33MHz or 64-bit/33MHz PCI Bus extensions. The PCI slots support the PCI Local Bus 2.1 Specification. Twelve of the PCI slots are on the secondary PCI Bus, which is implemented using three Intel PCI-to-PCI bridges. The remaining four PCI slots are on the tertiary PCI Bus, which is implemented using a fourth Intel PCI-to-PCI bridge.

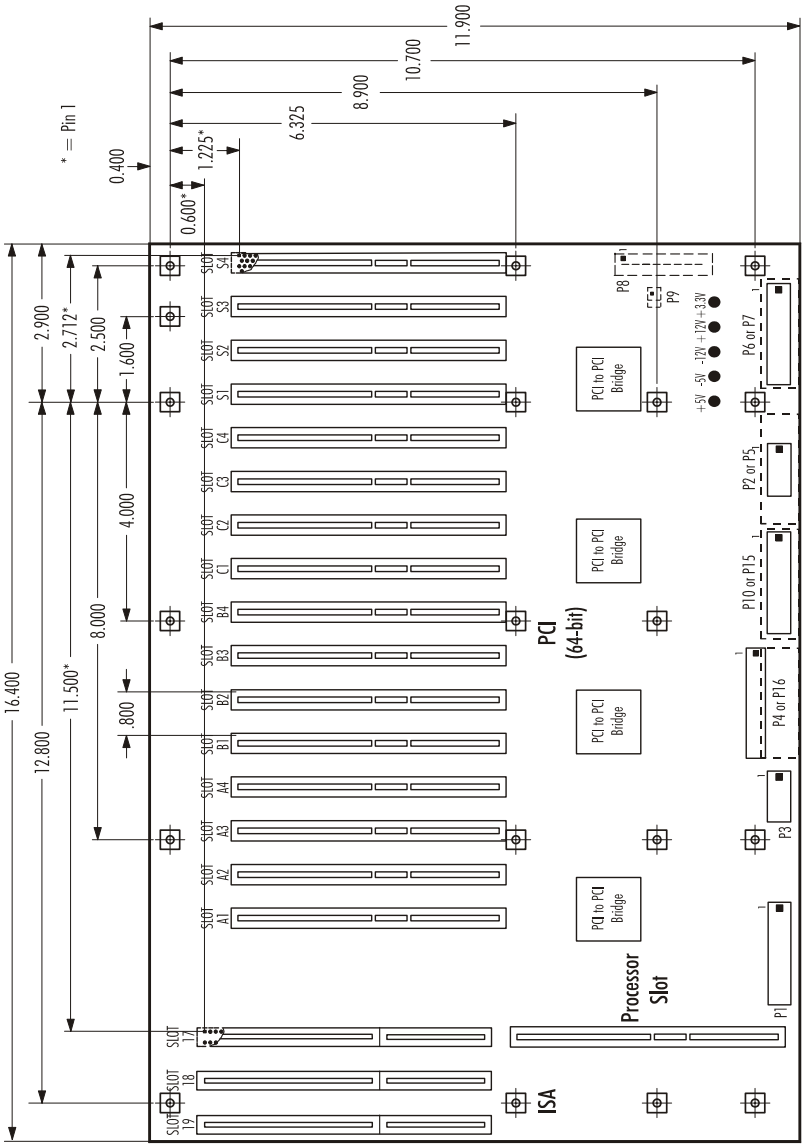
The standard AT power connection is available through two 12-pin .156 MTA connectors or one terminal block connector. Power connection for +3.3V is available through a 12-pin .156 MTA connector or an ATX connector (optional).

An extended-current option is also available. The extended-current connectors provide additional power capacity for power-intensive applications -- up to 150 Amps of +5V plus 150 Amps of +3.3V.

5696-000
BP3/16-64
BUS DIAGRAM



5696-000
BP3/16-64
DIMENSIONAL DRAWING



PCB thickness .062”
Mounting holes .156” diameter
Connector spacing .800” centers

5696-000 BP3/16-64 CONNECTORS

NOTE: Pin 1 on the connectors is indicated by the square pad on the PCB.

P1 - Power Supply Connector
12 pin right angle, Molex #26-60-5120

Pin	Signal
1	NC
2	+5V
3	+12V
4	-12V
5	Gnd
6	Gnd
7	Gnd
8	Gnd
9	-5V
10	+5V
11	+5V
12	+5V

P2 - +5V Extended-Current Connector (optional)
5 pin right angle, Amp #193839-4
31 Amps per circuit
(Refer to Amp Doc. #108-1594)

Pin	Signal
1	+5V
2	+5V
3	+5V
4	+5V
5	+5V

P3 - Auxiliary Power Supply Connector
6 pin right angle, Molex #26-60-5060

Pin	Signal
1	+5V
2	+5V
3	+5V
4	Gnd
5	Gnd
6	Gnd

5696-000
BP3/16-64
CONNECTORS (CONTINUED)

P4 - Alternate Power Supply Connector
10 position terminal block, Augat #2MV-10
20 Amps per circuit

Pin	Signal
1	+5V
2	+5V
3	+5V
4	Gnd
5	Gnd
6	Gnd
7	Gnd
8	-5V
9	-12V
10	+12V

P5 - Auxiliary Power Supply Connector
6 pin right angle, Molex #26-60-5060

Pin	Signal
1	+5V
2	+5V
3	+5V
4	Gnd
5	Gnd
6	Gnd

P6 - Power Supply Connector
12 pin right angle, Molex #26-60-5120

Pin	Signal
1	NC
2	+5V
3	+12V
4	-12V
5	Gnd
6	Gnd
7	Gnd
8	Gnd
9	-5V
10	+5V
11	+5V
12	+5V

5696-000
BP3/16-64
CONNECTORS (CONTINUED)

P7 - +5V Return Extended-Current Connector (optional)
5 pin right angle, Amp #193839-4
31 Amps per circuit
(Refer to Amp Doc. #108-1594)

Pin	Signal
1	Gnd
2	Gnd
3	Gnd
4	Gnd
5	Gnd

P8 - ATX Connector (optional)
20 pin dual row header, Molex #39-29-9202

Pin	Signal	Pin	Signal
1	+3.3V	11	+3.3V
2	+3.3V	12	-12V
3	Gnd	13	Gnd
4	+5V	14	PS-ON
5	Gnd	15	Gnd
6	+5V	16	Gnd
7	Gnd	17	Gnd
8	PW-OK	18	-5V
9	+5VSB	19	+5V
10	+12V	20	+5V

P9 - ATX Power-On Connector (optional)
2 pin header, Amp #640456-2

Pin	Signal
1	PS-ON
2	Gnd

P10 - +3.3V Power Supply Connector
12 pin right angle, Molex #26-60-5120

Pin	Signal
1	+3.3V
2	+3.3V
3	+3.3V
4	Gnd
5	Gnd
6	Gnd
7	Gnd
8	Gnd
9	Gnd
10	+3.3V
11	+3.3V
12	+3.3V

5696-000
BP3/16-64
CONNECTORS
(CONTINUED)

P15 - +3.3V Extended-Current Connector (optional)
5 pin right angle, Amp #193839-4
31 Amps per circuit
(Refer to Amp Doc. #108-1594)

Pin	Signal
1	+3.3V
2	+3.3V
3	+3.3V
4	+3.3V
5	+3.3V

P16 - +3.3V Return Extended-Current Connector (optional)
5 pin right angle, Amp #193839-4
31 Amps per circuit
(Refer to Amp Doc. #108-1594)

Pin	Signal
1	Gnd
2	Gnd
3	Gnd
4	Gnd
5	Gnd

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5786-000
BP13/2/4-66

The BP13/2/4-66 is a PICMG-compatible backplane. It is a six-layer .062" thick PCB which provides 12 ISA slots, a 64-bit/66MHz SBC slot and six PCI Local Bus slots for use by standard PCI Local Bus option cards.

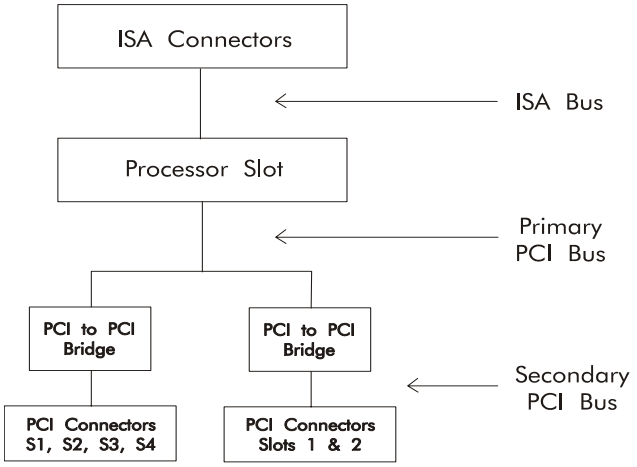
Of the six PCI Local Bus slots, two are 64-bit/66MHz PCI option slots and four are 64-bit/33MHz PCI option slots. Either 64-bit or 32-bit SBCs and option cards may be used. 64-bit and/or 66MHz option cards can take advantage of the 64-bit and/or 66MHz architecture when communicating with each other, even if a 32-bit SBC is used.

The PCI slots support the PCI Local Bus 2.1 Specification. Two of the PCI slots are on a secondary PCI Bus and are 64-bit/66MHz. These are +3.3V 64-bit PCI connectors on the backplane. Four of the PCI slots are 64-bit/33MHz and are on a secondary PCI Bus. These are +5V 64-bit PCI connectors on the backplane.

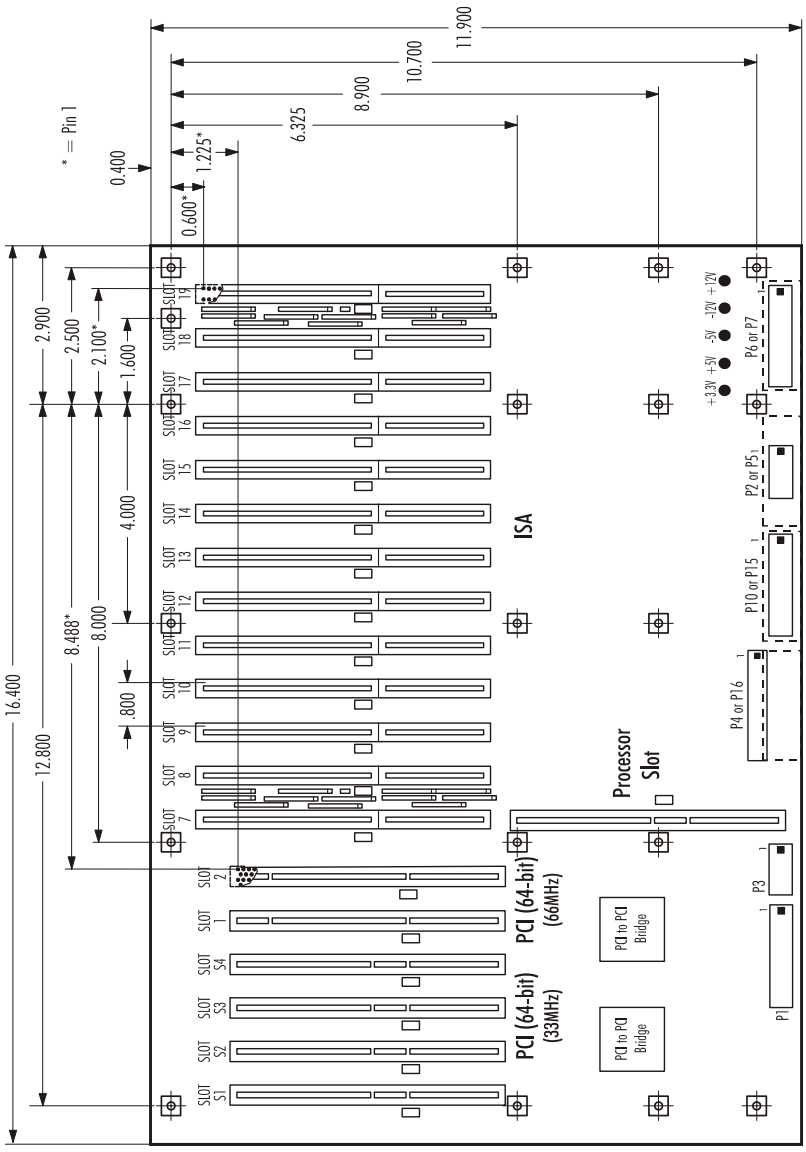
The standard AT power connection is available through two 12-pin .156 MTA connectors or one terminal block connector. Power connection for +3.3V is available through a 12-pin .156 MTA connector.

An extended-current option is also available. The extended-current connectors provide additional power capacity for power-intensive applications -- up to 150 Amps of +5V plus 150 Amps of +3.3V.

5786-000
BP13/2/4-66
BUS DIAGRAM



5786-000
BP13/2/4-66
DIMENSIONAL DRAWING



PCB thickness .062”
Mounting holes .156” diameter
Connector spacing .800” centers

5786-000
BP13/2/4-66
CONNECTORS

NOTE: Pin 1 on the connectors is indicated by the square pad on the PCB.

P1 - Power Supply Connector
12 pin right angle, Molex #26-60-5120

Pin	Signal
1	NC
2	+5V
3	+12V
4	-12V
5	Gnd
6	Gnd
7	Gnd
8	Gnd
9	-5V
10	+5V
11	+5V
12	+5V

P2 - +5V Extended-Current Connector (optional)
5 pin right angle, Amp #193839-4
31 Amps per circuit
(Refer to Amp Doc. #108-1594)

Pin	Signal
1	+5V
2	+5V
3	+5V
4	+5V
5	+5V

P3 - Auxiliary Power Supply Connector
6 pin right angle, Molex #26-60-5060

Pin	Signal
1	+5V
2	+5V
3	+5V
4	Gnd
5	Gnd
6	Gnd

5786-000
BP13/2/4-66
CONNECTORS (CONTINUED)

P4 - Alternate Power Supply Connector
10 position terminal block, Augat #2MV-10
20 Amps per circuit

Pin	Signal
1	+5V
2	+5V
3	+5V
4	Gnd
5	Gnd
6	Gnd
7	Gnd
8	-5V
9	-12V
10	+12V

P5 - Auxiliary Power Supply Connector
6 pin right angle, Molex #26-60-5060

Pin	Signal
1	+5V
2	+5V
3	+5V
4	Gnd
5	Gnd
6	Gnd

P6 - Power Supply Connector
12 pin right angle, Molex #26-60-5120

Pin	Signal
1	NC
2	+5V
3	+12V
4	-12V
5	Gnd
6	Gnd
7	Gnd
8	Gnd
9	-5V
10	+5V
11	+5V
12	+5V

5786-000
BP13/2/4-66
CONNECTORS (CONTINUED)

P7 - +5V Return Extended-Current Connector (optional)
5 pin right angle, Amp #193839-4
31 Amps per circuit
(Refer to Amp Doc. #108-1594)

Pin	Signal
1	Gnd
2	Gnd
3	Gnd
4	Gnd
5	Gnd

P10 - +3.3V Power Supply Connector
12 pin right angle, Molex #26-60-5120

Pin	Signal
1	+3.3V
2	+3.3V
3	+3.3V
4	Gnd
5	Gnd
6	Gnd
7	Gnd
8	Gnd
9	Gnd
10	+3.3V
11	+3.3V
12	+3.3V

P15 - +3.3V Return Extended-Current Connector (optional)
5 pin right angle, Amp #193839-4
31 Amps per circuit
(Refer to Amp Doc. #108-1594)

Pin	Signal
1	Gnd
2	Gnd
3	Gnd
4	Gnd
5	Gnd

5786-000
BP13/2/4-66
CONNECTORS (CONTINUED)

P16 - +3.3V Extended-Current Connector (optional)
5 pin right angle, Amp #193839-4
31 Amps per circuit
(Refer to Amp Doc. #108-1594)

Pin	Signal
1	+3.3V
2	+3.3V
3	+3.3V
4	+3.3V
5	+3.3V

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5951-000
BP3/2/4/4

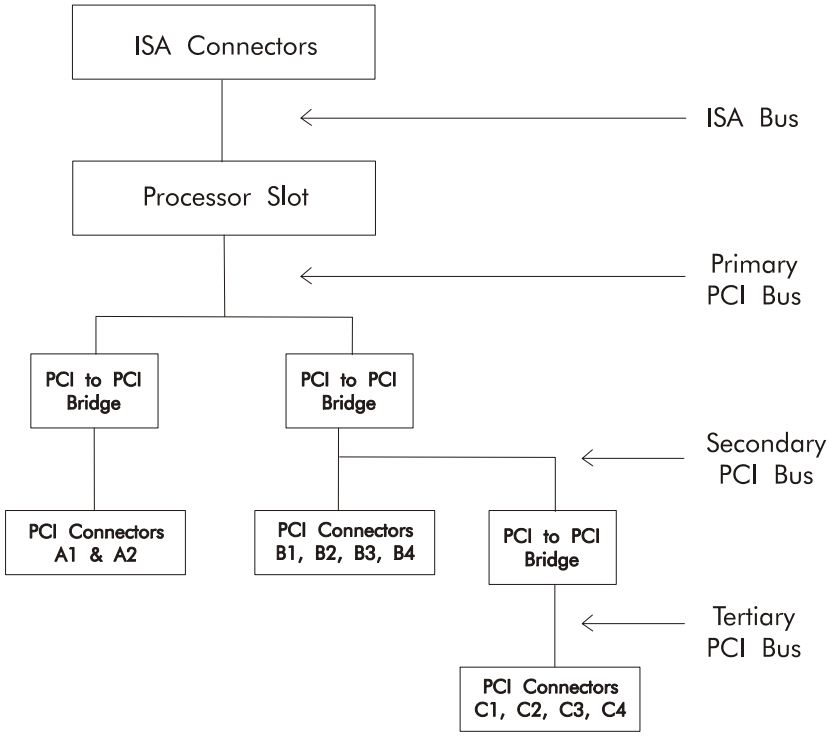
The BP3/2/4/4 is a PICMG-compatible backplane. It is a six-layer .062" thick PCB which provides two ISA slots, a 64-bit/66MHz SBC slot and ten PCI Local Bus slots for use by standard PCI Local Bus option cards.

Of the ten PCI Local Bus slots, two are 64-bit/66MHz PCI option slots, four are 64-bit/33MHz PCI option slots and four are 32-bit/33MHz PCI option slots. Either 64-bit or 32-bit SBCs and option cards may be used. 64-bit and/or 66MHz option cards can take advantage of the 64-bit and/or 66MHz architecture when communicating with each other, even if a 32-bit SBC is used.

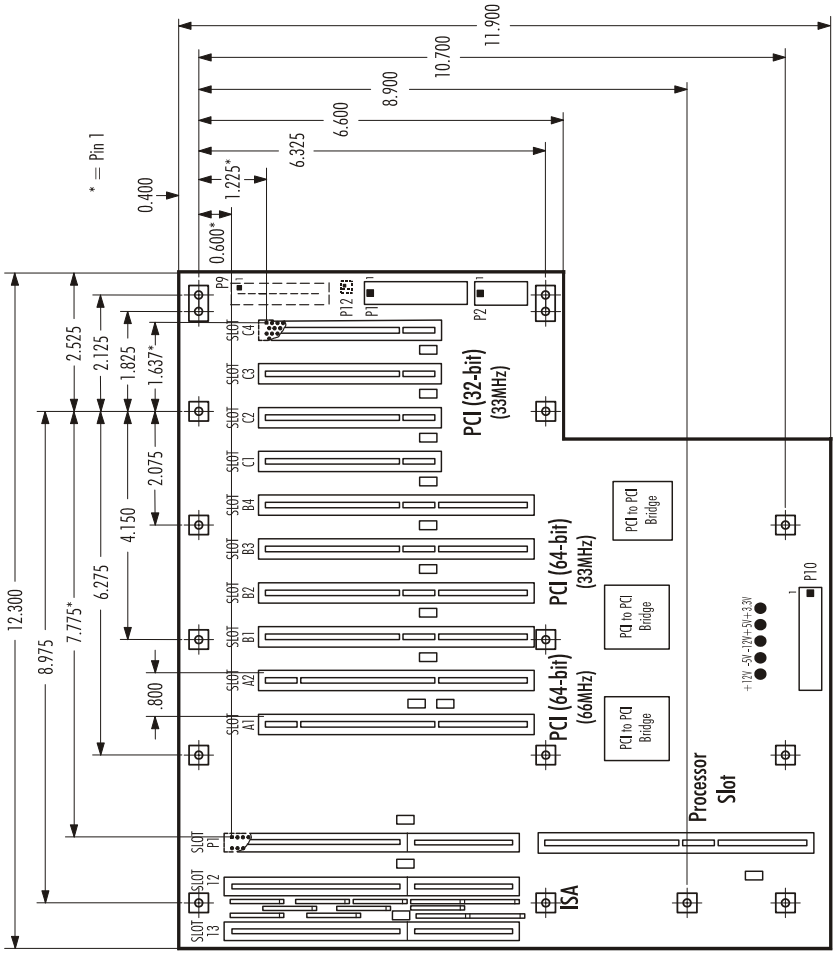
The PCI slots support the PCI Local Bus 2.1 Specification. Two of the PCI slots are on a secondary PCI Bus and are 64-bit/66MHz. These are +3.3V 64-bit PCI connectors on the backplane. Four of the PCI slots are 64-bit/33MHz and are on a secondary PCI Bus. These are +5V 64-bit PCI connectors on the backplane. Four of the PCI slots are 32-bit/33MHz and are on a tertiary PCI Bus. These are +5V 32-bit PCI connectors on the backplane.

The standard AT power connection is available through a 12-pin AT-style connector. Power connection for +3.3V is available through a 12-pin .156 MTA connector or an ATX connector (optional).

5951-000
BP3/2/4/4
BUS DIAGRAM



5951-000
BP3/2/4/4
DIMENSIONAL DRAWING



PCB thickness .062”
Mounting holes .156” diameter
Connector spacing .800” centers

5951-000 BP3/2/4/4 CONNECTORS

NOTE: Pin 1 on the connectors is indicated by the square pad on the PCB.

P1 - Power Supply Connector
12 pin single row header, Leoco #4301P12V000

Pin	Signal
1	NC
2	+5V
3	+12V
4	-12V
5	Gnd
6	Gnd
7	Gnd
8	Gnd
9	-5V
10	+5V
11	+5V
12	+5V

P2 - Auxiliary Power Supply Connector
6 pin single row header, Burndy #GTC6R-1

Pin	Signal
1	+5V
2	+5V
3	+5V
4	Gnd
5	Gnd
6	Gnd

P9 - ATX Connector (optional)
20 pin dual row header, Molex #39-29-9202

Pin	Signal	Pin	Signal
1	+3.3V	11	+3.3V
2	+3.3V	12	-12V
3	Gnd	13	Gnd
4	+5V	14	PS-ON
5	Gnd	15	Gnd
6	+5V	16	Gnd
7	Gnd	17	Gnd
8	PW-OK	18	-5V
9	+5VSB	19	+5V
10	+12V	20	+5V

5951-000 BP3/2/4/4 CONNECTORS (CONTINUED)

P10 - +3.3V Power Supply Connector
12 pin right angle, Molex #26-60-5120

Pin	Signal
1	+3.3V
2	+3.3V
3	+3.3V
4	Gnd
5	Gnd
6	Gnd
7	Gnd
8	Gnd
9	Gnd
10	+3.3V
11	+3.3V
12	+3.3V

P12 - ATX Power-On Connector (optional)
2 pin header, Amp #640456-2

Pin	Signal
1	PS-ON
2	Gnd

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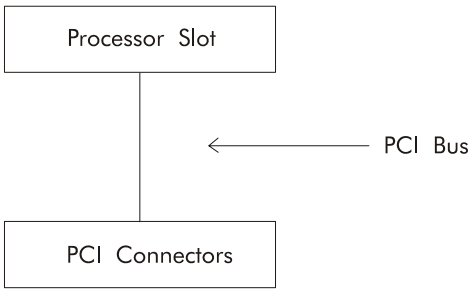
5971-000
BP1/2

The BP1/2 is a PICMG-compatible backplane. It is a six-layer .062" thick PCB which provides one 64-bit/33MHz SBC slot and two PCI Local Bus slots for use by standard PCI Local Bus option cards.

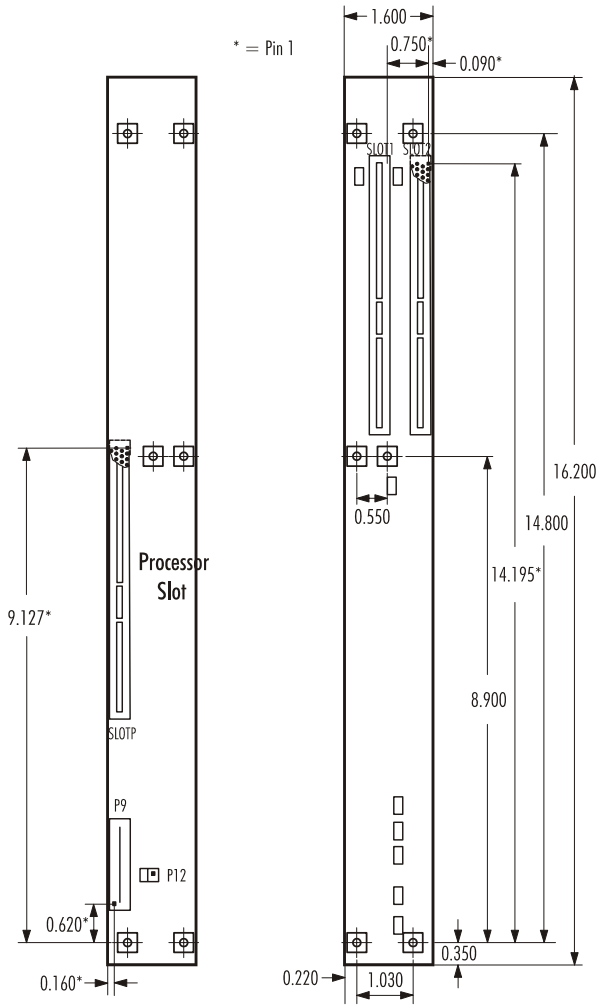
The two PCI slots are 64-bit/33MHz PCI option slots which support the PCI Local Bus 2.1 Specification. Either 64-bit or 32-bit SBCs and option cards may be used.

Power connection is available through an ATX connector.

5971-000
BP1/2
BUS DIAGRAM



5971-000
BP1/2
DIMENSIONAL
DRAWING



PCB thickness .062”
Mounting holes .156” diameter
Connector spacing .800” centers

5971-000 BP1/2 CONNECTORS

NOTE: Pin 1 on the connectors is indicated by the square pad on the PCB.

P9 - ATX Connector
20 pin dual row header, Molex #39-29-9202

Pin	Signal	Pin	Signal
1	+3.3V	11	+3.3V
2	+3.3V	12	-12V
3	Gnd	13	Gnd
4	+5V	14	PS-ON
5	Gnd	15	Gnd
6	+5V	16	Gnd
7	Gnd	17	Gnd
8	PW-OK	18	-5V
9	+5VSB	19	+5V
10	+12V	20	+5V

P12 - ATX Power-On Connector
2 pin header, Amp #640456-2

Pin	Signal
1	PS-ON
2	Gnd

6195-000
BP3/6/4

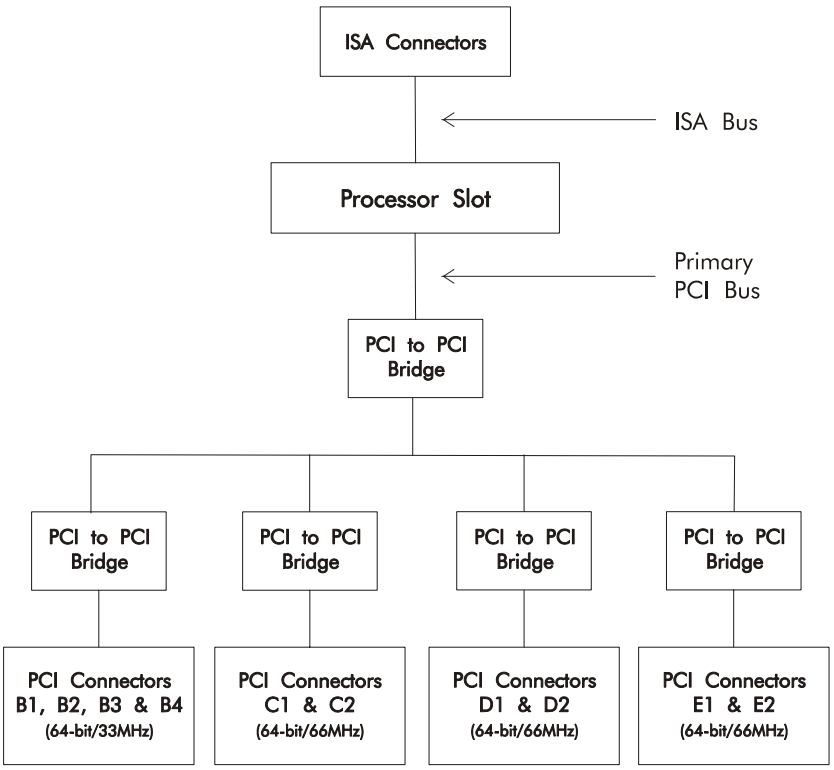
The BP3/6/4 is a PICMG-compatible backplane. It is a six-layer .062" thick PCB which provides two ISA slots, a 64-bit/66MHz SBC slot and ten PCI Local Bus slots for use by standard PCI/ISA option cards.

Of the ten PCI Local Bus slots, six are 64-bit/66MHz PCI option slots and four are 64-bit/33MHz PCI option slots. Either 64-bit or 32-bit SBCs and option cards may be used. 64-bit and/or 66MHz option cards can take advantage of the 64-bit and/or 66MHz architecture when communicating with each other, even if a 32-bit SBC is used.

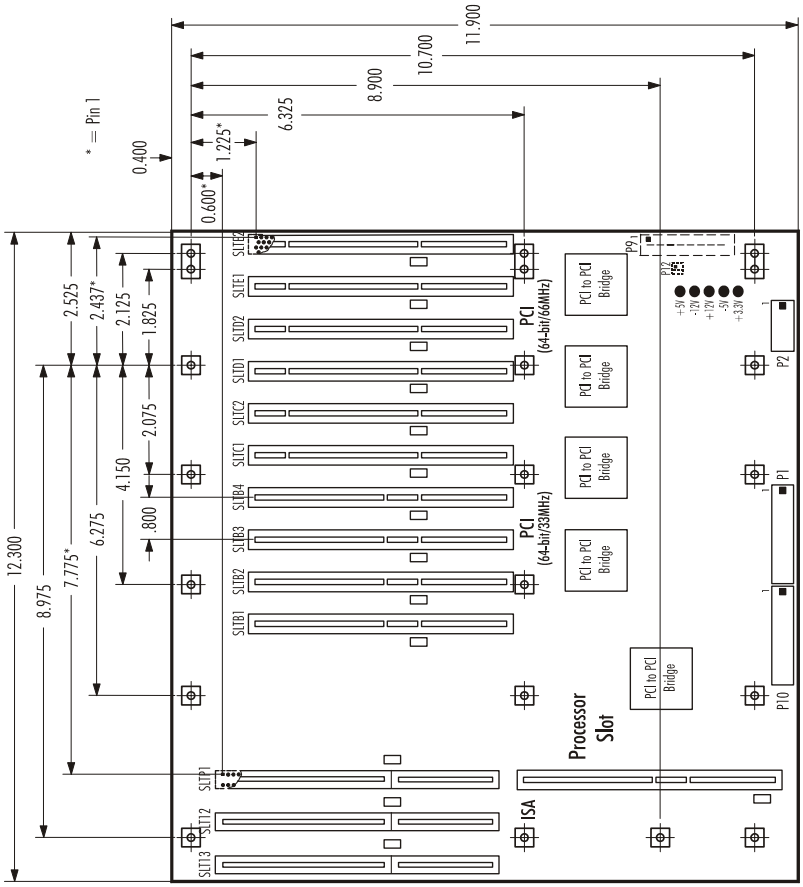
The PCI slots support the PCI Local Bus 2.1 Specification. The six 64-bit/66MHz PCI slots are +3.3V 64-bit PCI connectors on the backplane and the four 64-bit/33MHz PCI slots are +5V 64-bit PCI connectors. A total of five Intel PCI-to-PCI bridges are used in the backplane's architecture.

The standard AT power connection is available through a 12-pin .156 MTA connector. Power connection for +3.3V is available through a 12-pin .156 MTA connector or an ATX connector (optional).

6195-000
BP3/6/4
BUS DIAGRAM



6195-000
BP3/6/4
DIMENSIONAL DRAWING



PCB thickness .062”
Mounting holes .156” diameter
Connector spacing .800” centers

6195-000
BP3/6/4
CONNECTORS

NOTE: Pin 1 on the connectors is indicated by the square pad on the PCB.

P1 - Power Supply Connector
12 pin right angle, Molex #26-60-5120

Pin	Signal
1	NC
2	+5V
3	+12V
4	-12V
5	Gnd
6	Gnd
7	Gnd
8	Gnd
9	-5V
10	+5V
11	+5V
12	+5V

P2 - Auxiliary Power Supply Connector
6 pin right angle, Molex #26-60-5060

Pin	Signal
1	+5V
2	+5V
3	+5V
4	Gnd
5	Gnd
6	Gnd

P9 - ATX Connector (optional)
20 pin dual row header, Molex #39-29-9202

Pin	Signal	Pin	Signal
1	+3.3V	11	+3.3V
2	+3.3V	12	-12V
3	Gnd	13	Gnd
4	+5V	14	PS-ON
5	Gnd	15	Gnd
6	+5V	16	Gnd
7	Gnd	17	Gnd
8	PW-OK	18	-5V
9	+5VSB	19	+5V
10	+12V	20	+5V

6195-000 BP3/6/4 CONNECTORS (CONTINUED)

P10 - +3.3V Power Supply Connector
12 pin right angle, Molex #26-60-5120

Pin	Signal
1	+3.3V
2	+3.3V
3	+3.3V
4	Gnd
5	Gnd
6	Gnd
7	Gnd
8	Gnd
9	Gnd
10	+3.3V
11	+3.3V
12	+3.3V

P12 - ATX Power-On Connector (optional)
2 pin header, Amp #640456-2

Pin	Signal
1	PS-ON
2	Gnd

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Chapter 5 Segmented Backplanes

5574-000
BP2S13

The BP2S13 is a 13-slot PICMG-compatible backplane. It is a six-layer .062" thick PCB which is divided into two segments, with each segment operating independently and consisting of an ISA Bus and a PCI Local Bus. The two segments share the same power source. All of the PCI Local Bus slots support the PCI Local Bus 2.1 Specification.

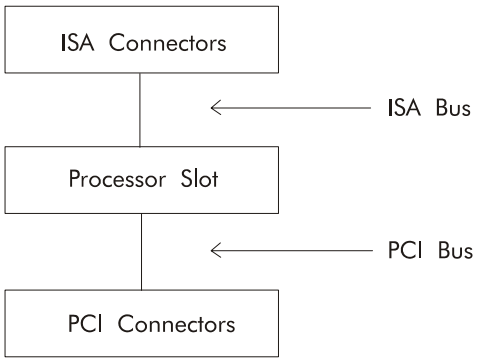
One of the segments provides one ISA slot which is dedicated to the SBC with PCI extension, three additional ISA Bus slots for the use of standard ISA Bus option cards and three PCI Local Bus slots for the use of standard PCI Local Bus option cards.

The other segment provides one ISA slot dedicated to the SBC with PCI extension, two additional ISA Bus slots and three PCI Local Bus slots.

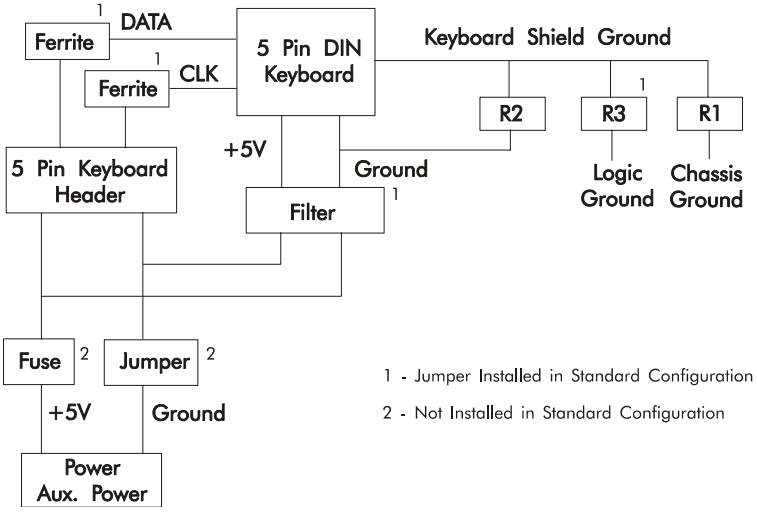
The standard AT power connection is available through a 12-pin AT-style connector or a terminal block connector. Power connection for +3.3V is available through a 12-pin AT-style connector or an ATX connector (optional).

5574-000
BP2S13
BUS DIAGRAM

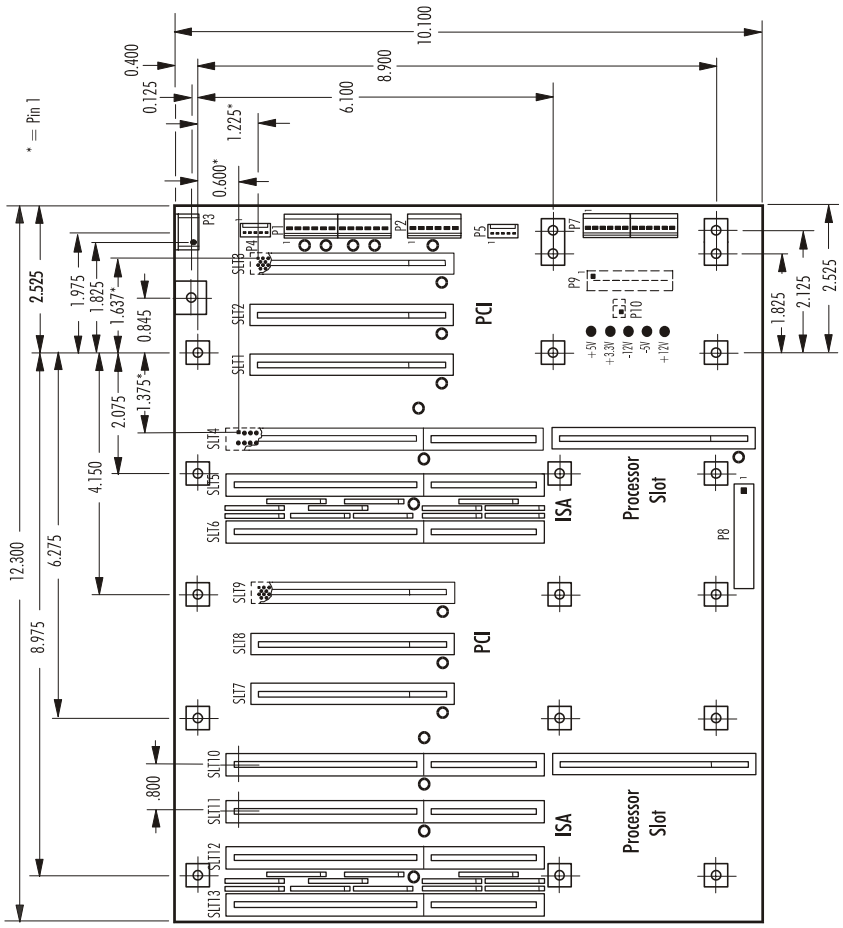
The following diagram applies to each segment of the backplane:



KEYBOARD DIAGRAM



5574-000
BP2S13
DIMENSIONAL DRAWING



PCB thickness .062”
Mounting holes .156” diameter
Connector spacing .800” centers

5574-000 BP2S13 CONNECTORS

NOTE: Pin 1 on the connectors is indicated by the square pad on the PCB.

P1 - Power Supply Connector
12 pin single row header, Leoco #4301P12V000

Pin	Signal
1	NC
2	+5V
3	+12V
4	-12V
5	Gnd
6	Gnd
7	Gnd
8	Gnd
9	-5V
10	+5V
11	+5V
12	+5V

P2 - Auxiliary Power Supply Connector
6 pin single row header, Burndy #GTC6R-1

Pin	Signal
1	+5V
2	+5V
3	+5V
4	Gnd
5	Gnd
6	Gnd

P3 - Keyboard Connector
5 pin DIN, Amp #520842-1

Pin	Signal
1	Kbd Clock
2	Kbd Data
3	NC
4	Kbd Gnd
5	Kbd Power (+5V fused)

P4 - Keyboard Connector
5 pin single row header, Amp #640456-5

Pin	Signal
1	Kbd Clock
2	Kbd Data
3	NC
4	Kbd Gnd
5	Kbd Power (+5V fused)

5574-000
BP2S13
CONNECTORS (CONTINUED)

P5 - Keyboard Connector
5 pin single row header, Amp #640456-5

Pin	Signal
1	Kbd Clock
2	Kbd Data
3	NC
4	Kbd Gnd
5	Kbd Power (+5V fused)

P7 - +3.3V Power Supply Connector
12 pin single row header, Leoco #4301P12V000

Pin	Signal
1	+3.3V
2	+3.3V
3	+3.3V
4	Gnd
5	Gnd
6	Gnd
7	Gnd
8	Gnd
9	Gnd
10	+3.3V
11	+3.3V
12	+3.3V

P8 - Alternate Power Supply Connector
10 position terminal block, Augat #2MV-10

Pin	Signal
1	+5V
2	+5V
3	+5V
4	Gnd
5	Gnd
6	Gnd
7	Gnd
8	-5V
9	-12V
10	+12V

P9 - ATX Connector (optional)
20 pin dual row header, Molex #39-29-9202

Pin	Signal	Pin	Signal
1	+3.3V	11	+3.3V
2	+3.3V	12	-12V
3	Gnd	13	Gnd

5574-000
BP2S13
CONNECTORS (CONTINUED)

P9 - ATX Connector (continued)

Pin	Signal	Pin	Signal
4	+5V	14	PS-ON
5	Gnd	15	Gnd
6	+5V	16	Gnd
7	Gnd	17	Gnd
8	PW-OK	18	-5V
9	+5VSB	19	+5V
10	+12V	20	+5V

P10 - ATX Power-On Connector (optional)
2 pin header, Amp #640456-2

Pin	Signal
1	PS-ON
2	Gnd

5577-000
BP2S19

The BP2S19 is a 19-slot PICMG-compatible backplane. It is a six-layer .062" thick PCB which is divided into two segments, with each segment operating independently and consisting of an ISA Bus and a PCI Local Bus. The two segments share the same power source. All of the PCI Local Bus slots support the PCI Local Bus 2.1 Specification.

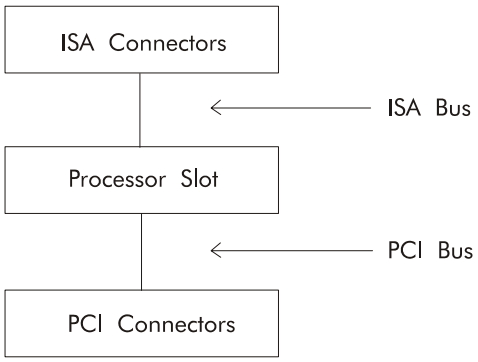
One of the segments provides one ISA slot which is dedicated to the SBC with PCI extension, six additional ISA Bus slots for the use of standard ISA Bus option cards and three PCI Local Bus slots for the use of standard PCI Local Bus option cards.

The other segment provides one ISA slot dedicated to the SBC with PCI extension, five additional ISA Bus slots and three PCI Local Bus slots.

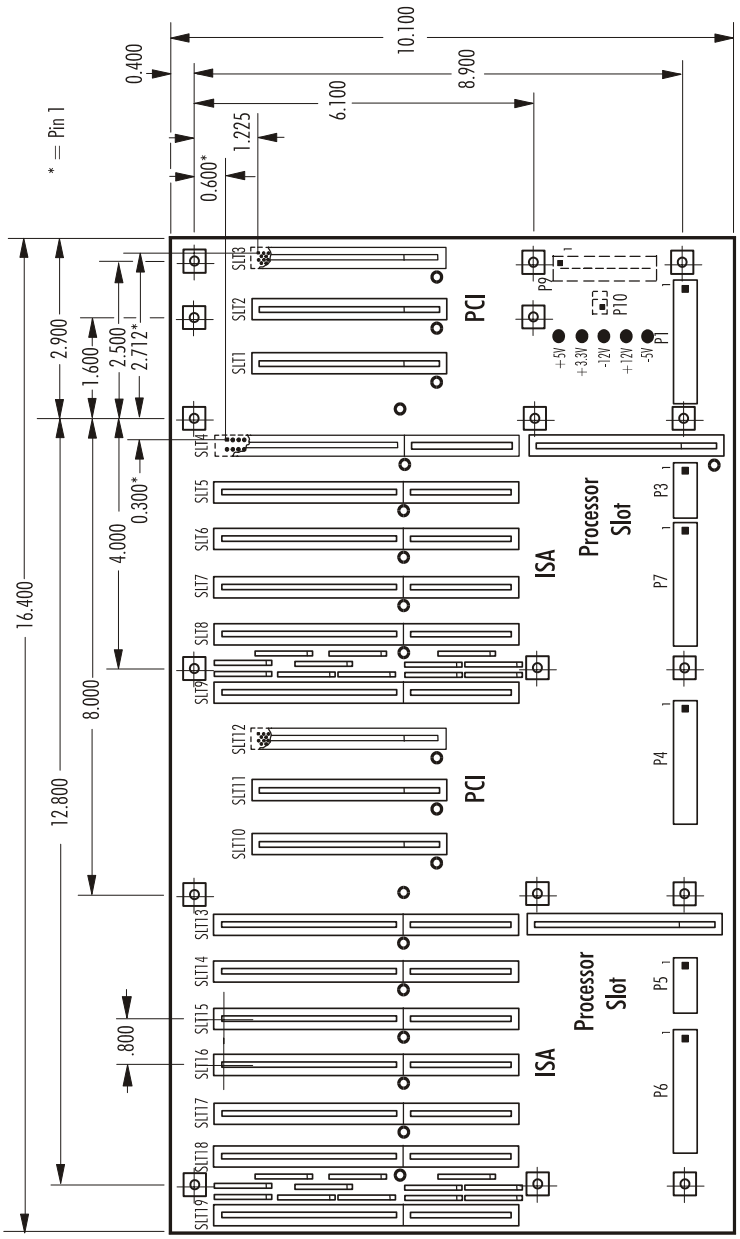
The standard AT power connection is available through two 12-pin .156 MTA connectors or one terminal block connector. Power connection for +3.3V is available through a 12-pin .156 MTA connector or an ATX connector (optional).

5577-000 BP2S19 BUS DIAGRAM

The following diagram applies to each segment of the backplane:



5577-000
BP2S19
DIMENSIONAL DRAWING



PCB thickness .062”
Mounting holes .156” diameter
Connector spacing .800” centers

5577-000
BP2S19
CONNECTORS

NOTE: Pin 1 on the connectors is indicated by the square pad on the PCB.

P1 - Power Supply Connector
12 pin right angle, Molex #26-60-5120

Pin	Signal
1	NC
2	+5V
3	+12V
4	-12V
5	Gnd
6	Gnd
7	Gnd
8	Gnd
9	-5V
10	+5V
11	+5V
12	+5V

P3 - Auxiliary Power Supply Connector
6 pin right angle, Molex #26-60-5060

Pin	Signal
1	+5V
2	+5V
3	+5V
4	Gnd
5	Gnd
6	Gnd

P4 - Alternate Power Supply Connector
10 position terminal block, Augat #2MV-10

Pin	Signal
1	+5V
2	+5V
3	+5V
4	Gnd
5	Gnd
6	Gnd
7	Gnd
8	-5V
9	-12V
10	+12V

5577-000
BP2S19
CONNECTORS (CONTINUED)

P5 - Auxiliary Power Supply Connector
6 pin right angle, Molex #26-60-5060

Pin	Signal
1	+5V
2	+5V
3	+5V
4	Gnd
5	Gnd
6	Gnd

P6 - Power Supply Connector
12 pin right angle, Molex #26-60-5120

Pin	Signal
1	NC
2	+5V
3	+12V
4	-12V
5	Gnd
6	Gnd
7	Gnd
8	Gnd
9	-5V
10	+5V
11	+5V
12	+5V

P7 - +3.3V Power Supply Connector
12 pin right angle, Molex #26-60-5120

Pin	Signal
1	+3.3V
2	+3.3V
3	+3.3V
4	Gnd
5	Gnd
6	Gnd
7	Gnd
8	Gnd
9	Gnd
10	+3.3V
11	+3.3V
12	+3.3V

5577-000
BP2S19
CONNECTORS (CONTINUED)

P9 - ATX Connector (optional)
20 pin dual row header, Molex #39-29-9202

Pin	Signal	Pin	Signal
1	+3.3V	11	+3.3V
2	+3.3V	12	-12V
3	Gnd	13	Gnd
4	+5V	14	PS-ON
5	Gnd	15	Gnd
6	+5V	16	Gnd
7	Gnd	17	Gnd
8	PW-OK	18	-5V
9	+5VSB	19	+5V
10	+12V	20	+5V

P10 - ATX Power-On Connector (optional)
2 pin header, Amp #640456-2

Pin	Signal
1	PS-ON
2	Gnd

Chapter 6 PCI-X Backplanes

6120-000
BP1/1/2/4/4

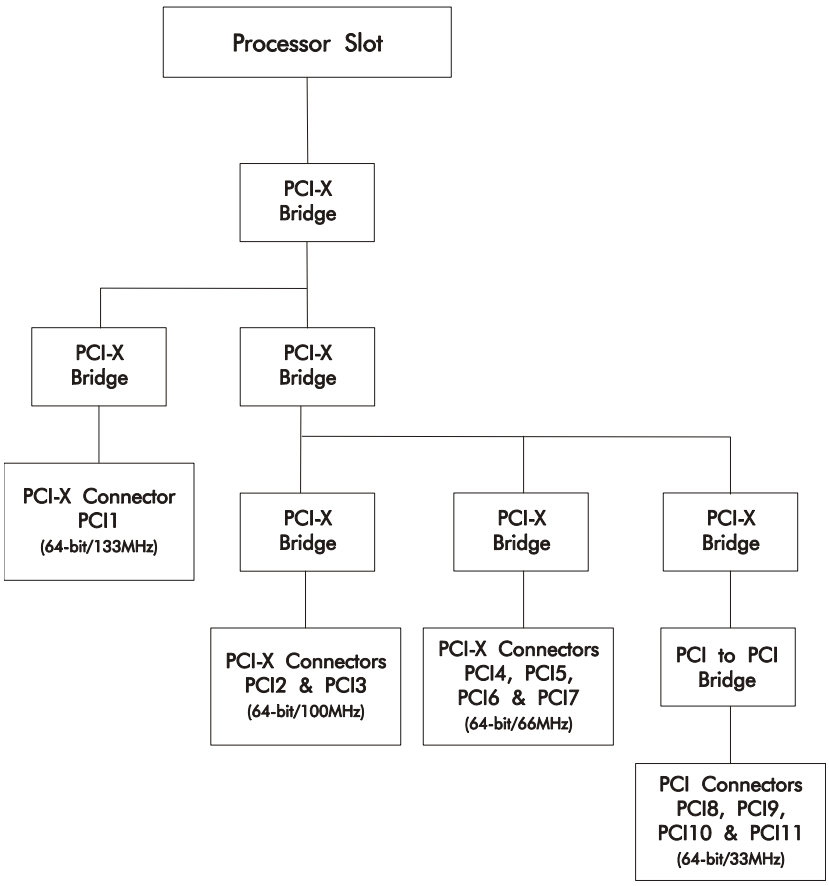
The BP1/1/2/4/4 is a PICMG-compatible backplane. It is an eight-layer .062" thick PCB which provides an SBC slot which can run up to 64-bit/133MHz and 11 PCI-X/PCI Local Bus slots for use by standard PCI-X and PCI option cards.

Of the 11 PCI-X/PCI Local Bus slots, one is a 64-bit/133MHz PCI-X option slot, two are 64-bit/100MHz PCI-X option slots, four are 64-bit/66MHz PCI-X option slots and four are 64-bit/33MHz PCI option slots.

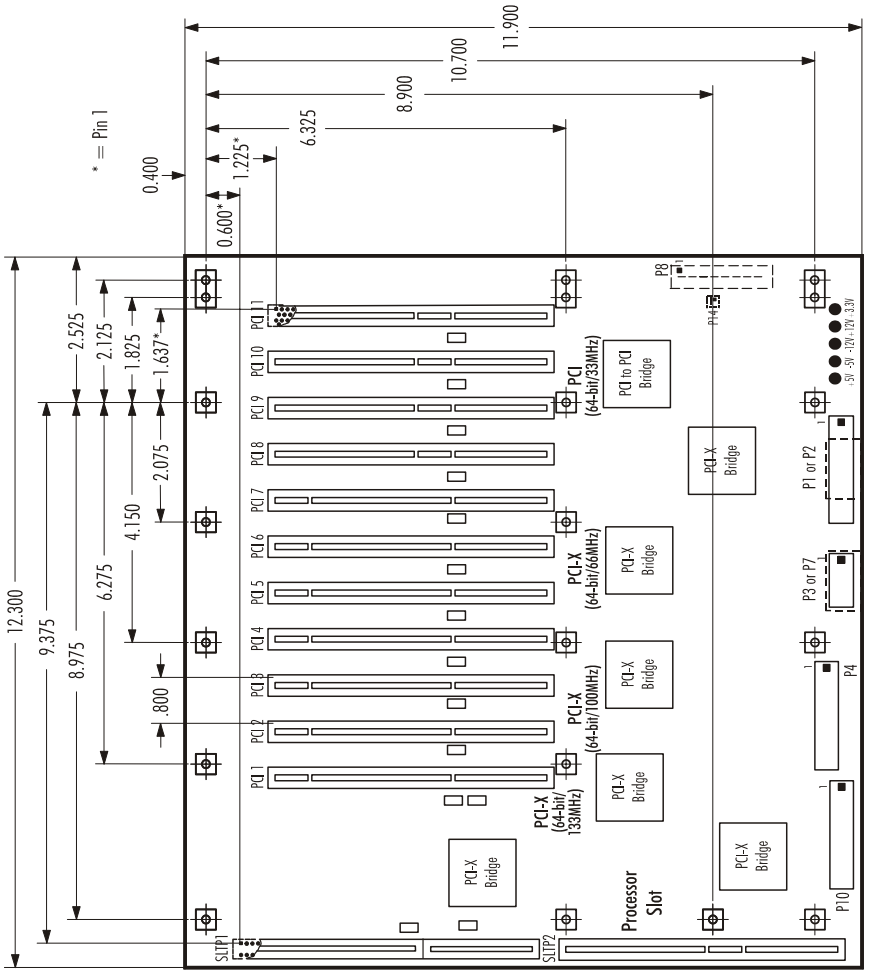
The standard AT power connection is available through a 12-pin .156 MTA connector. Power connection for +3.3V is available through a 12-pin .156 MTA connector or an ATX connector (optional).

An extended-current option is also available. The extended-current connectors provide additional power capacity for power-intensive applications -- up to 60 Amps of +5V plus 60 Amps of +3.3V.

6120-000
BP1/1/2/4/4
BUS DIAGRAM



6120-000
BP1/1/2/4/4
DIMENSIONAL DRAWING



PCB thickness .062”
Mounting holes .156” diameter
Connector spacing .800” centers

6120-000 BP1/1/2/4/4 CONNECTORS

NOTE: Pin 1 on the connectors is indicated by the square pad on the PCB.

P1 - Power Supply Connector
12 pin right angle, Molex #26-60-5120

Pin	Signal
1	NC
2	+5V
3	+12V
4	-12V
5	Gnd
6	Gnd
7	Gnd
8	Gnd
9	-5V
10	+5V
11	+5V
12	+5V

P2 - Extended-Current Connector (optional)
4 pin right angle, Amp #193839-3
31 Amps per circuit

Pin	Signal
1	+3.3V
2	Gnd
3	Gnd
4	+5V

P3 - Auxiliary Power Supply Connector
6 pin right angle, Molex #26-60-5060

Pin	Signal
1	+5V
2	+5V
3	+5V
4	Gnd
5	Gnd
6	Gnd

P4 - Alternate Power Supply Connector
10 position terminal block, Augat #2MV-10
20 Amps per circuit

Pin	Signal
1	+5V
2	+5V
3	+5V
4	Gnd

6120-000 BP1/1/2/4/4 CONNECTORS (CONTINUED)

P4 - Alternate Power Supply Connector (continued)

Pin	Signal
5	Gnd
6	Gnd
7	Gnd
8	-5V
9	-12V
10	+12V

P7 - Extended-Current Connector (optional)
4 pin right angle, Amp #193839-3
31 Amps per circuit

Pin	Signal
1	+3.3V
2	Gnd
3	Gnd
4	+5V

P8 - ATX Connector (optional)
20 pin dual row header, Molex #39-29-9202

Pin	Signal	Pin	Signal
1	+3.3V	11	+3.3V
2	+3.3V	12	-12V
3	Gnd	13	Gnd
4	+5V	14	PS-ON
5	Gnd	15	Gnd
6	+5V	16	Gnd
7	Gnd	17	Gnd
8	PW-OK	18	-5V
9	+5VSB	19	+5V
10	+12V	20	+5V

P10 - +3.3V Power Supply Connector
12 pin right angle, Molex #26-60-5120

Pin	Signal
1	+3.3V
2	+3.3V
3	+3.3V
4	Gnd
5	Gnd
6	Gnd
7	Gnd
8	Gnd
9	Gnd

6120-000 BP1/1/2/4/4 CONNECTORS (CONTINUED)

P10 - +3.3V Power Supply Connector (continued)

Pin	Signal
10	+3.3V
11	+3.3V
12	+3.3V

P14 - ATX Power-On Connector (optional)
2 pin header, Amp #640456-2

Pin	Signal
1	PS-ON
2	Gnd